

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
DDRIII DIMMA1&DDRIII DIMMB1	7,8
LYNX PCIE/DMI/USB/CLK	9
LYNX-SATA/HOST/FAN/GPIO/VGA	10
LYNX-SMB/LPC/AUDIO/RTC	11
LYNX -POWER/GND/STRAPS	12,13,14
Dual BIOS/CLK Buffer_9DB433/CLK_GEN49325	15,16,17
MCU/PCIE SLOT	18~22
ALC1150/USB3.0 HUB/PCIE HUB/USB3.1	23~28
ASM3.0/LAN /USB HOTKEY/dischage	29,30,32
GPIO CONTROLLER/USB CHARGE F75501	33,34
REAR IO USB3.0 CONNECTOR	35,36,37
WIFI +BT/DISPLAY/HDMI CONNECTOR	38,39,40
FRONT CONNECTOROR(INTEL/ASM/M2/SATA)	41~44
SIO6792/CLR_CMOS	45,46,47
FAN CONTROLLER	48,49
Over votoltage/ACPI/ATX/BUTTON	50~53
VR12.5-PWM ISL6388+ISL6611	54,55
VCORE PHASE 1~12	56,57,58
DDR Power -uP1606PQ	59
12VIN CURRENT SENSE	60
LYNX PWR - MPS NB675	61
EMI CAP/Manial Part/XDP CPU & PCH	62,63,64
Power Map/Power Sequence/GPIO MAP	65,66,67
Revision History	68

MS-7888

ATX:243*305

Ver: 11

Intel -SharkBay plamform (Z97-MPOWER-MAX)

CPU:

Haswell-R LGA1150

*CPU POWER PAK *12 Phase*

System Chipset:

Lynx Point Z97

Onboard Chip:

HD Audio Codec:ALC1150

LAN-INTEL-I218V

SIO:NCT6792D

Flash ROM: SPI 64 MB X2

ASM1061-SATA6G-2Port

CLK Buffer: IDT9DB433

CLK GEN: IDT6V49325

WiFi / BT: Rear IO Pinheader

USB Hotkey: FinteK F75501

USB Charge: SLG55583A

USB3.0 HUB: ASM1074X2

PCIE HUB: ASM1184e

MCU:LPC812

USB3.1:ASM1142e

Main Memory:

*DDRIII * 4 (Dual Channel)*

ACPI:

UPI-uP7501+uP1714

Expansion Slots:

*PCI Express (X16) Slot * 3*

*PCI Express (X1) Slot * 4*

PWM:

VCORE VRD12.5 -

PWM-ISL6388+ISL6611

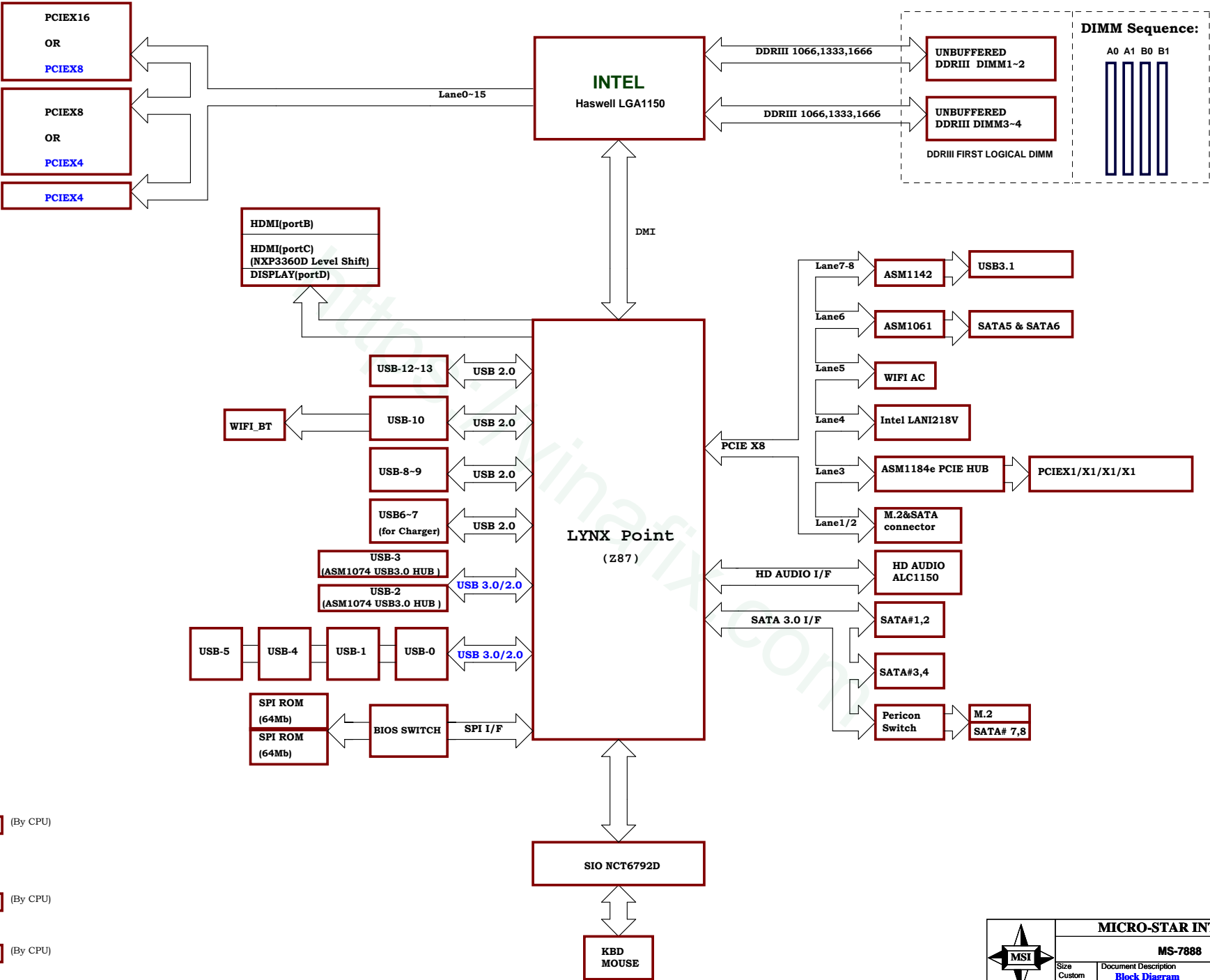
DDR -UPI1606 - 2Phase

PCH(1.05V) -MPS NB675



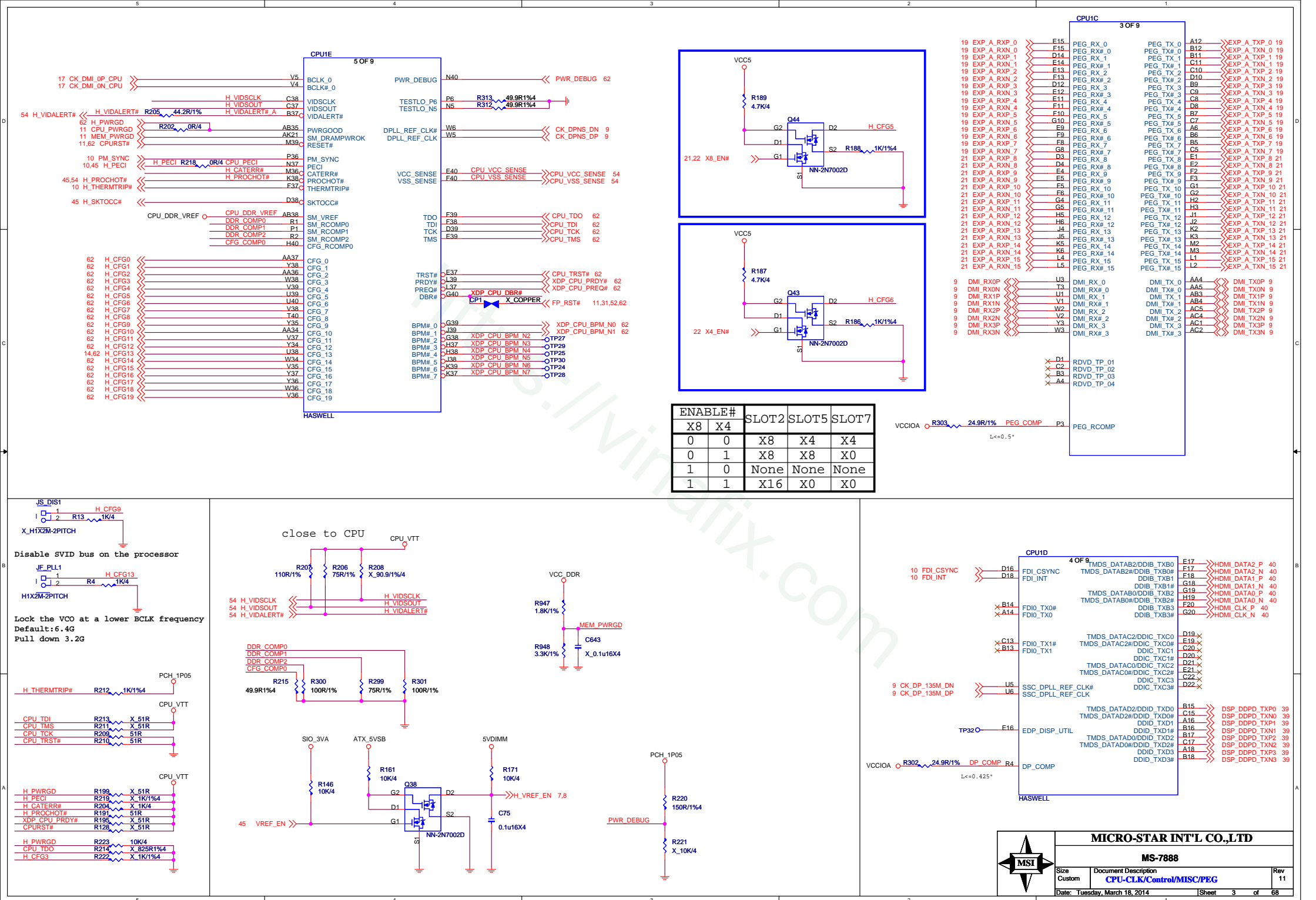
MICRO-STAR INT'L CO.,LTD		
MS-7888		
Size Custom	Document Description Cover Sheet	Rev 11
Date: Tuesday, March 18, 2014	Sheet 1 of 68	

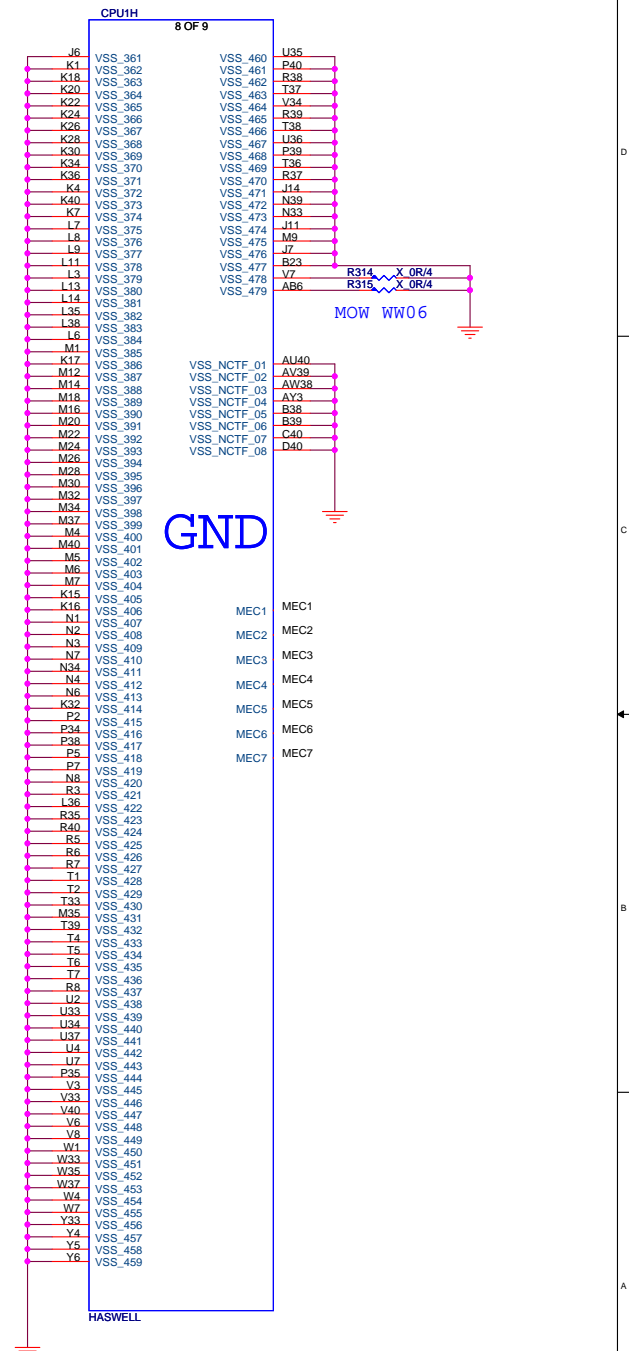
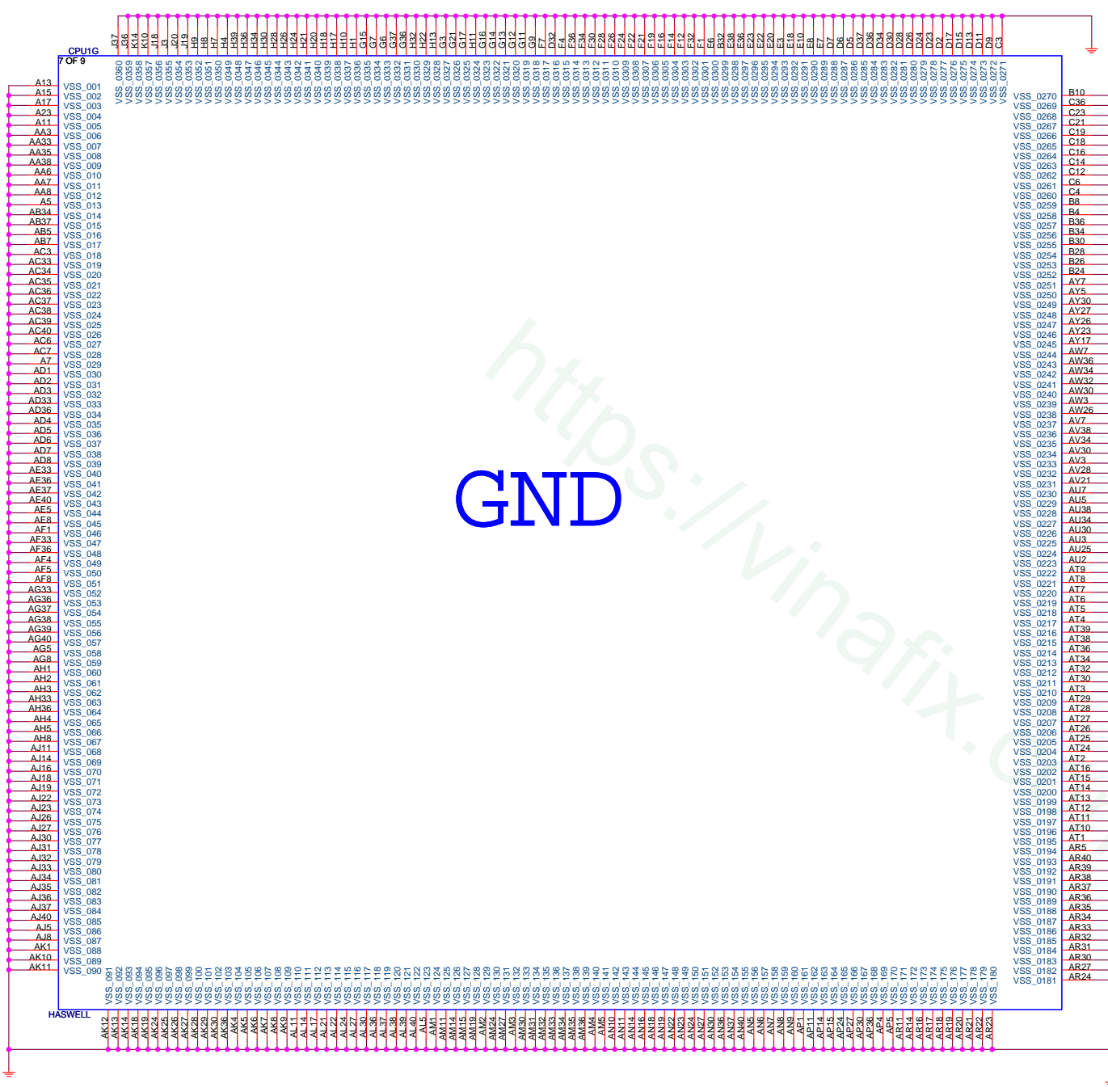
MS-7888 0A Block Diagram

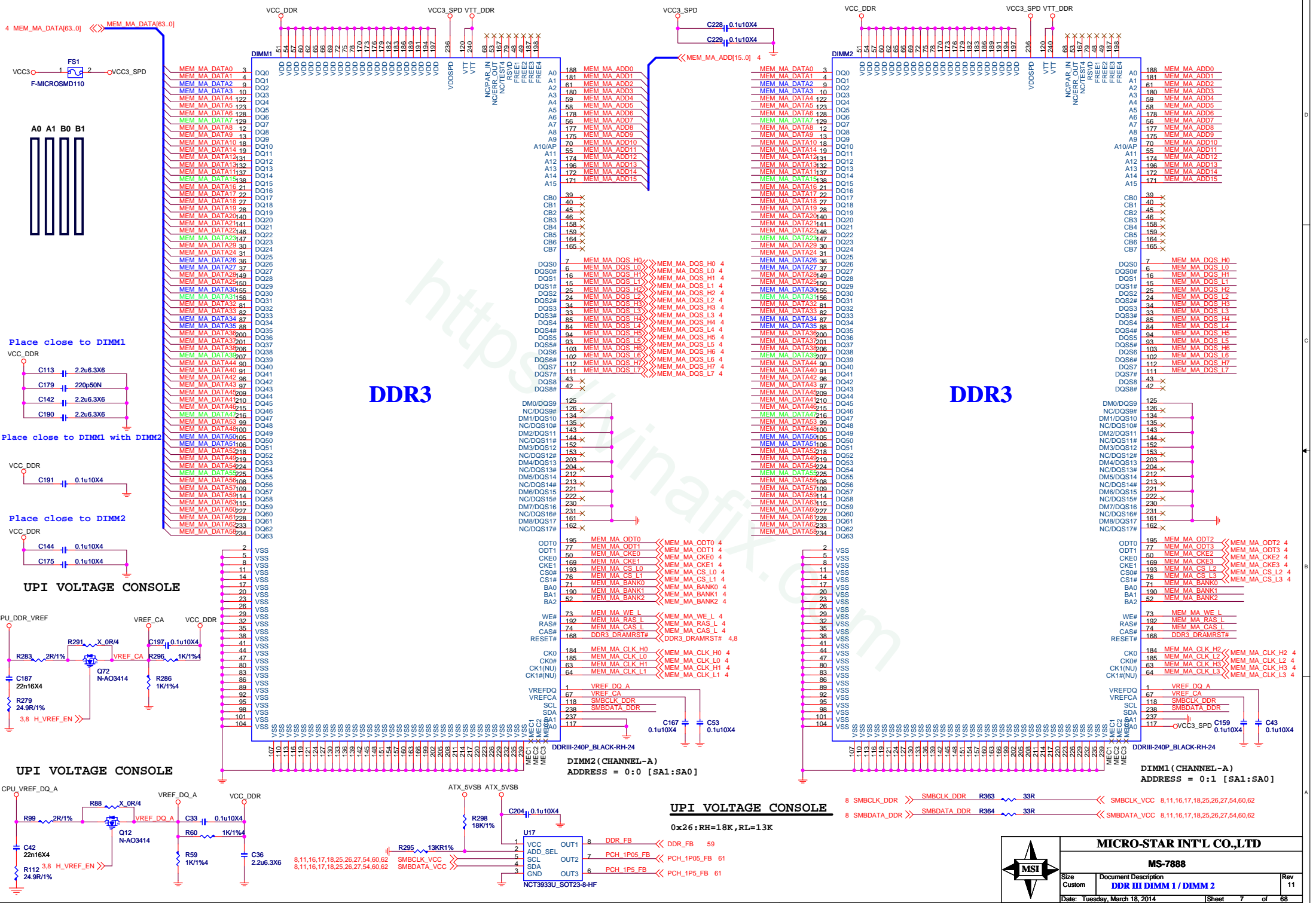


Slot Sequence:

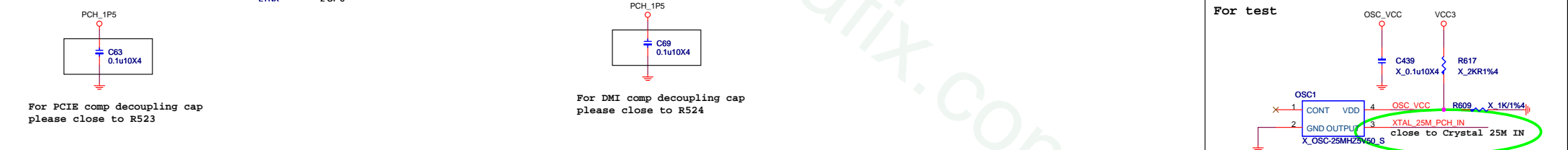
PCIE X1	
PCIE X16/X8/X8	(By CPU)
PCIE X1	
PCIE X1	
PCIE X0/ X8/X4	(By CPU)
PCIE X1	
PCIE X0/X0/X4	(By CPU)





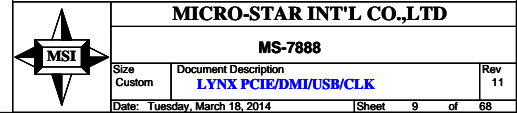
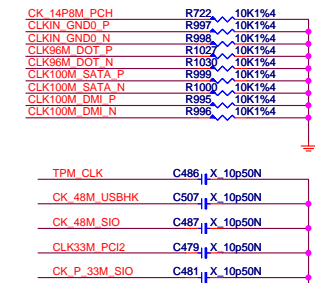


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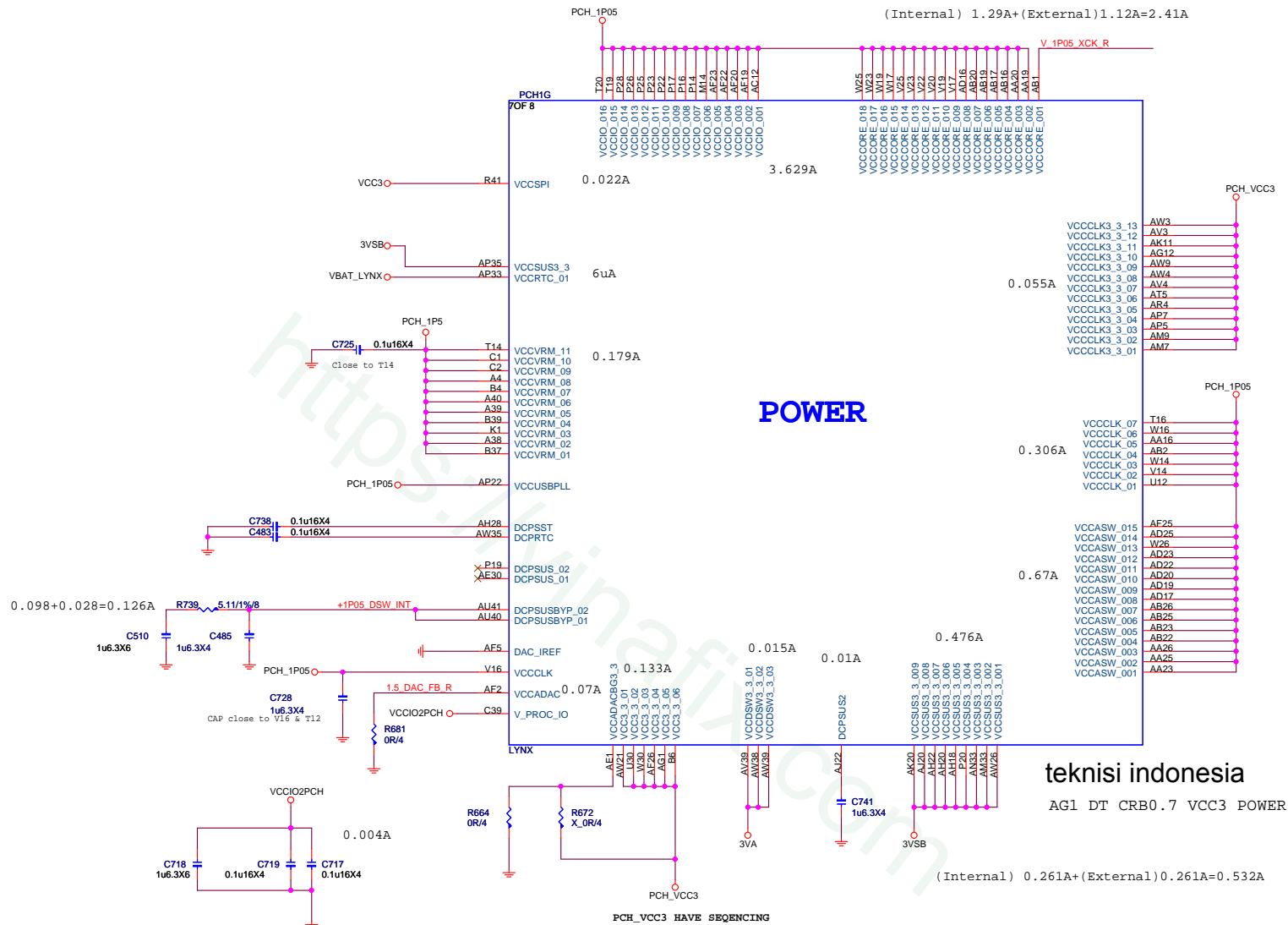
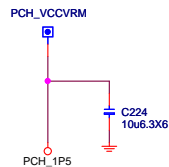
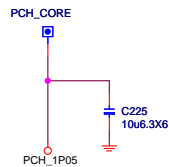
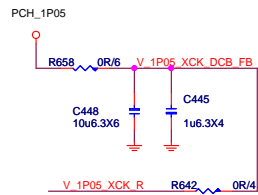
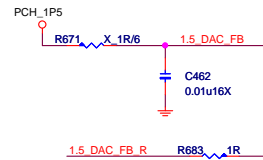


For PCIe comp decoupling cap
please close to R523

For DMI comp decoupling cap
please close to R524



Change to 10UH if
VCCA_DPLLA/VCCA_DPLL B
has noise issue.

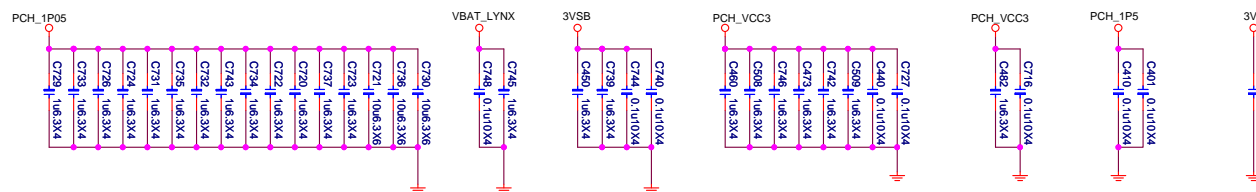


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AG1 DT CRB0.7 VCC3 POWER

(Internal) 0.261A+(External) 0.261A=0.532A

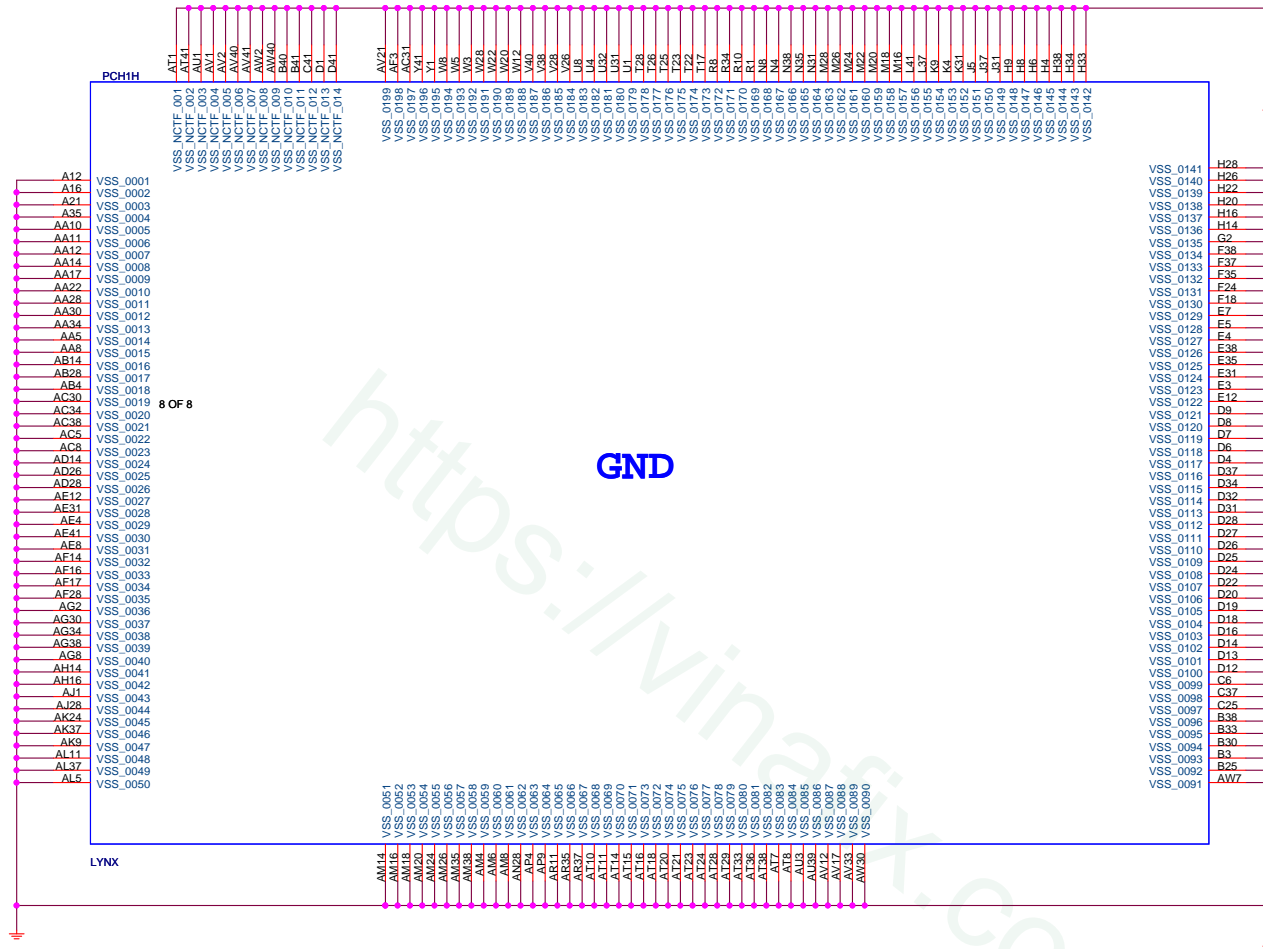
PCH decoupling cap

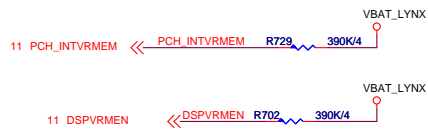
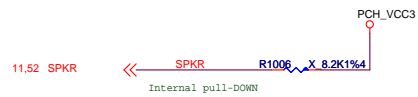


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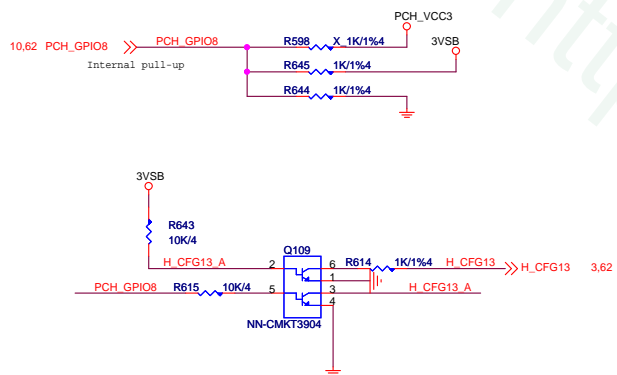
MS-7888

Size	Document Description	Rev
Custom	LYNX -POWER PIN	11
Date: Tuesday, March 18, 2014	Sheet 12 of 68	



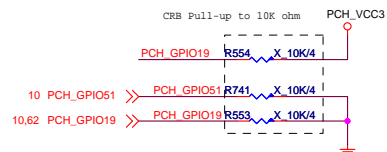


GPIO8



GPIO19 & GPIO51

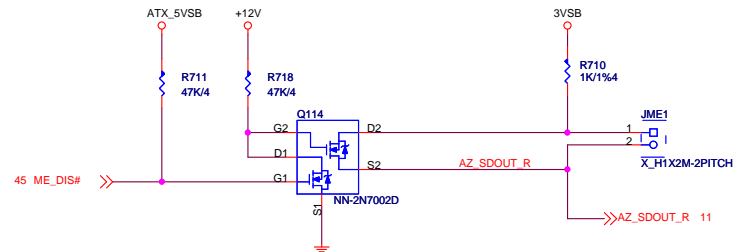
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1



Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO55

TOP BLOOCK SWAP MODE



GPIO55
Default Mode:
Internal pull-up.

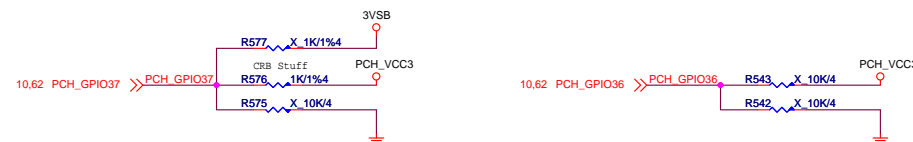
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

GPIO53



GPIO53
Connect to ground with 1k Ohm pull-down resistor.

GPIO36 & GPIO37

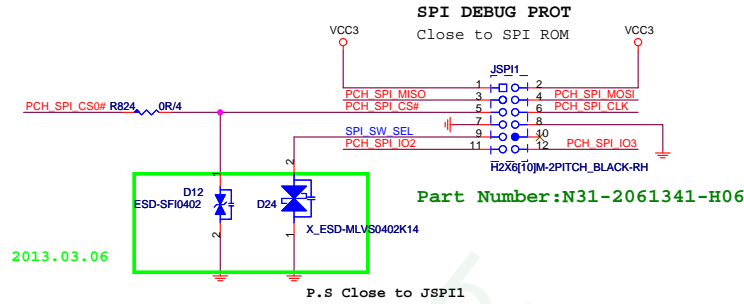


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MS-7888

Size	Document Description	Rev
Custom	LYNX STRAPS	11
Date:	Tuesday, March 18, 2014	Sheet 14 of 68

11 PCH_SPI_CS0# << PCH_SPI_CS0#
 11 PCH_SPI_MOSI << PCH_SPI_MOSI
 11 PCH_SPI_MISO << PCH_SPI_MISO
 11 PCH_SPI_CLK << PCH_SPI_CLK
 11 PCH_SPI_IO2 << PCH_SPI_IO2
 11 PCH_SPI_IO3 << PCH_SPI_IO3

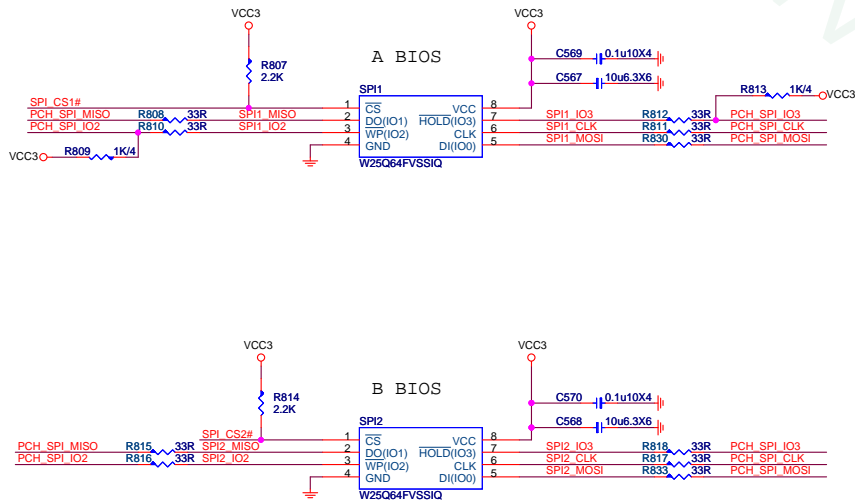


SPI FLASH ROM

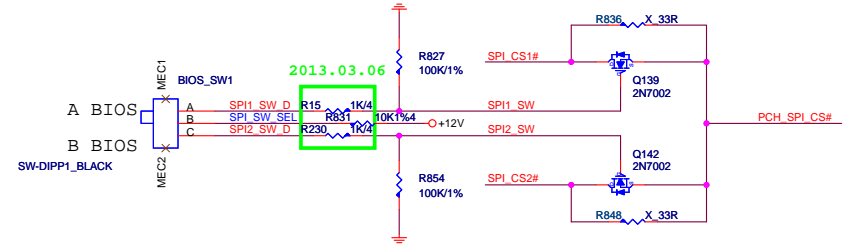
Place close to SB.

*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
 *SPI_CLK & SPI_CS0# must be length matched to within 500mils.

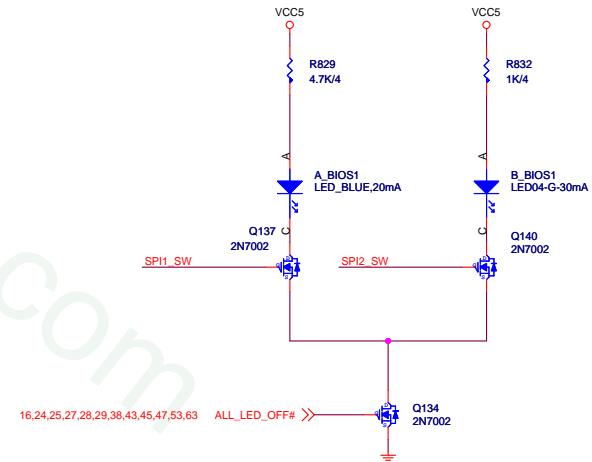
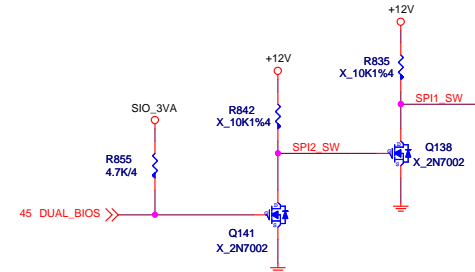
< 6 inch



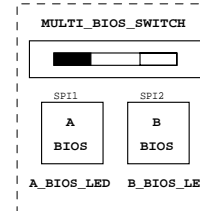
HW MODE



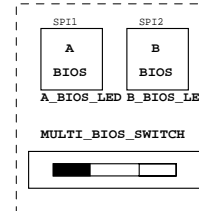
BIOS MODE



Placement 1



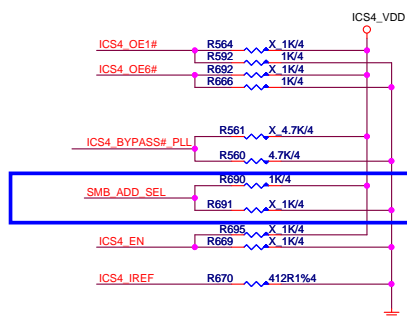
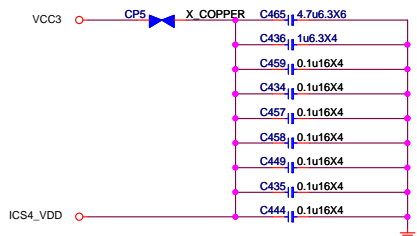
Placement 2



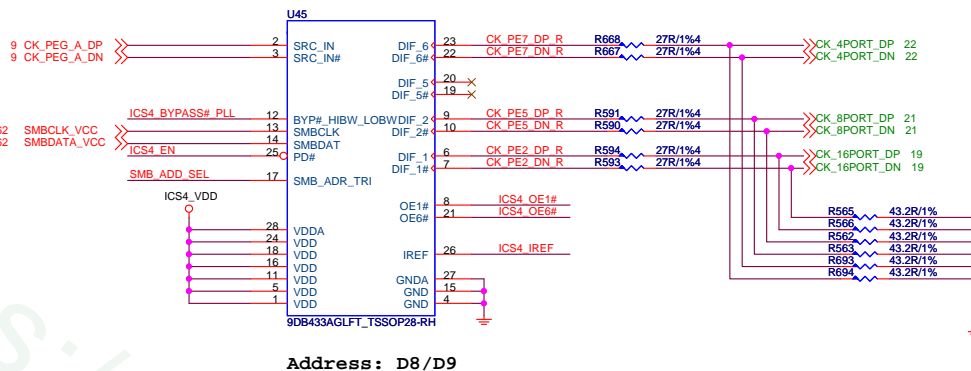
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MS-7888

Size Custom Document Description Dual BIOS Rev 11
 Date: Tuesday, March 18, 2014 Sheet 15 of 68

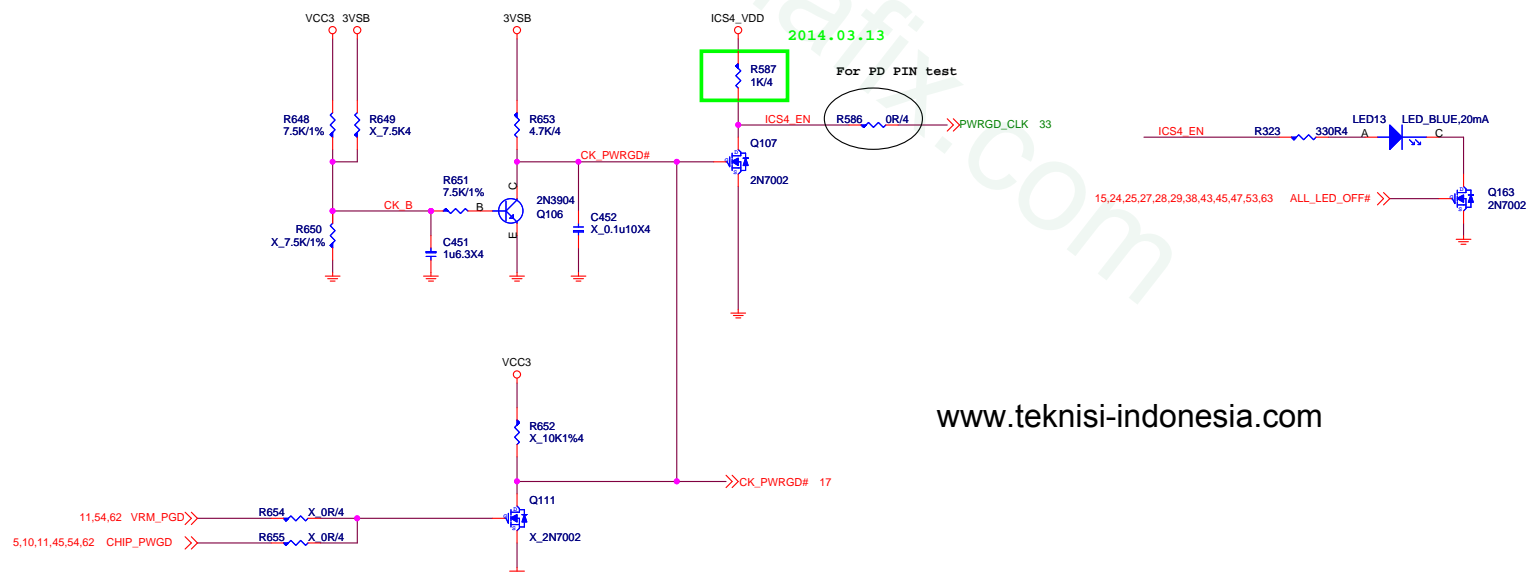


HIGH Address: D8/D9
LOW Address: DA/DB

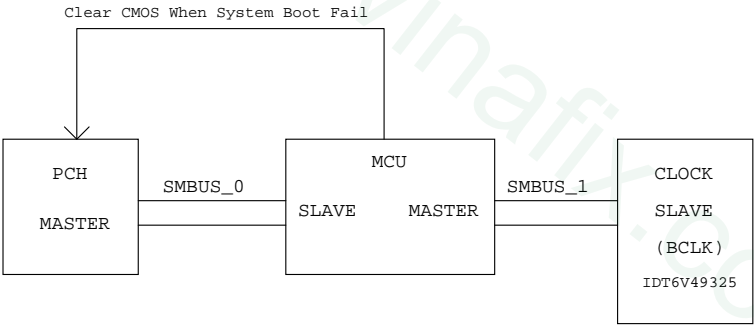
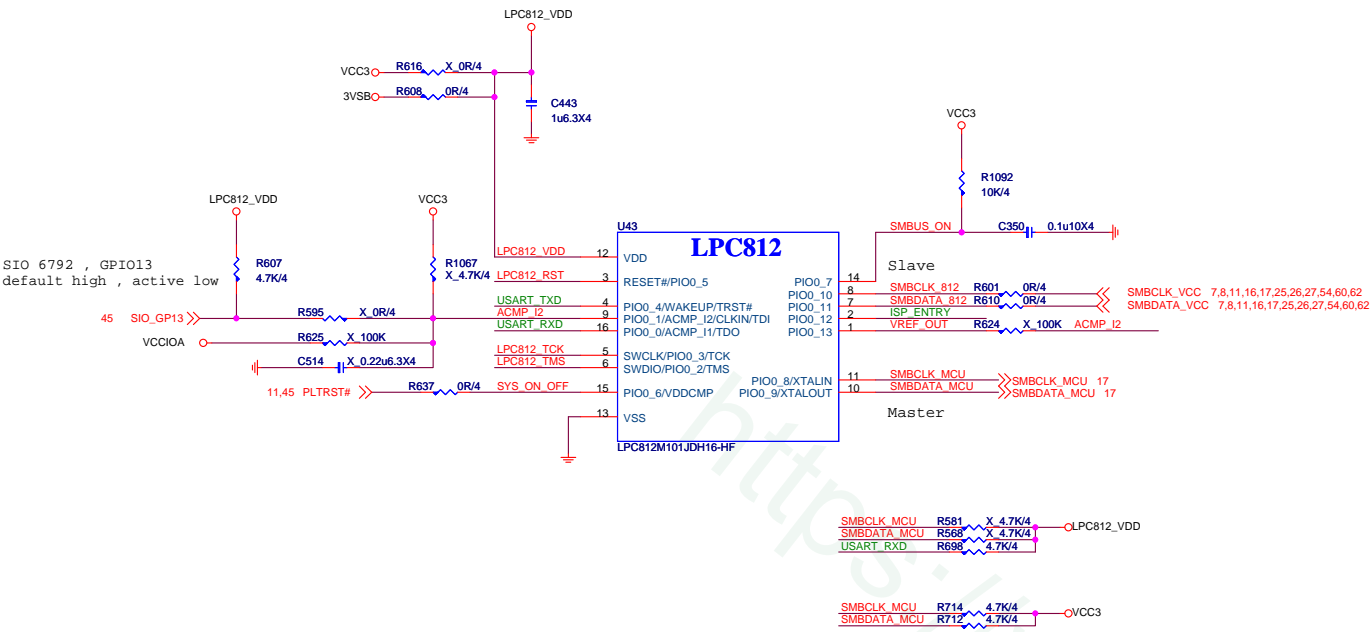


For PCIE Clock Jitter Issue

Address: D8/D9



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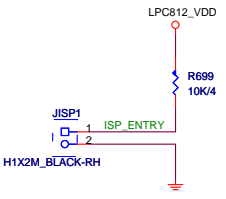


21.4 Pin description

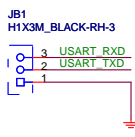
When the ISP entry pin is pulled LOW on reset, the part enters ISP mode and the ISP command handler starts up. In ISP mode, pin PIO0_0 is connected to function U0_RXD and pin PIO0_4 is connected to function U0_TXD on the USART0 block.

Table 232. Pin location in ISP mode					
ISP entry pin	USART RXD	USART TXD	Marking	Boot loader version	Package
PIO0_1	PIO0_0	PIO0_4	1A	v 13.1	TSSOP20; SO20; TSSOP16; DIP8
PIO0_1	PIO0_0	PIO0_4	2A	v 13.2	TSSOP20; SO20; TSSOP16; DIP8
PIO0_1	PIO0_0	PIO0_4	4C and later	v 13.4 and later	DIP8
PIO0_12	PIO0_0	PIO0_4	4C and later	v 13.4 and later	TSSOP20; SO20; TSSOP16

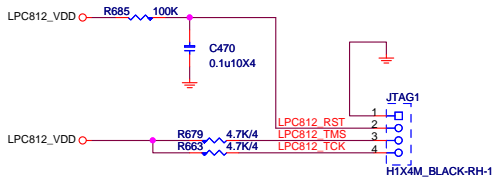
ENABLE ISP to FLASH

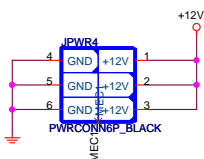
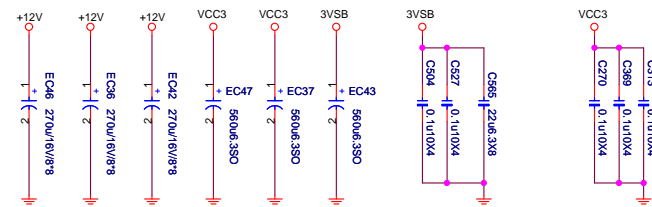
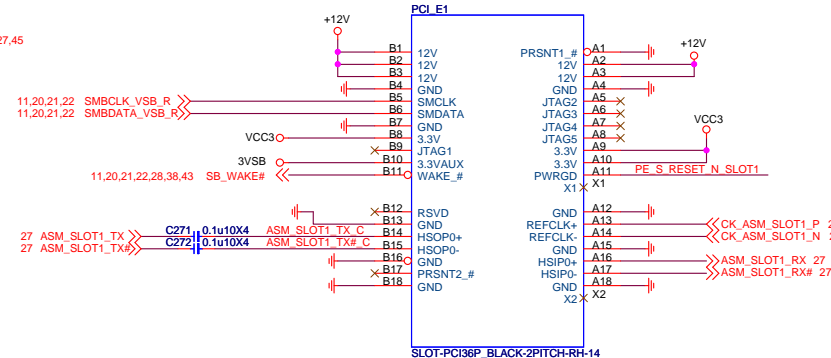
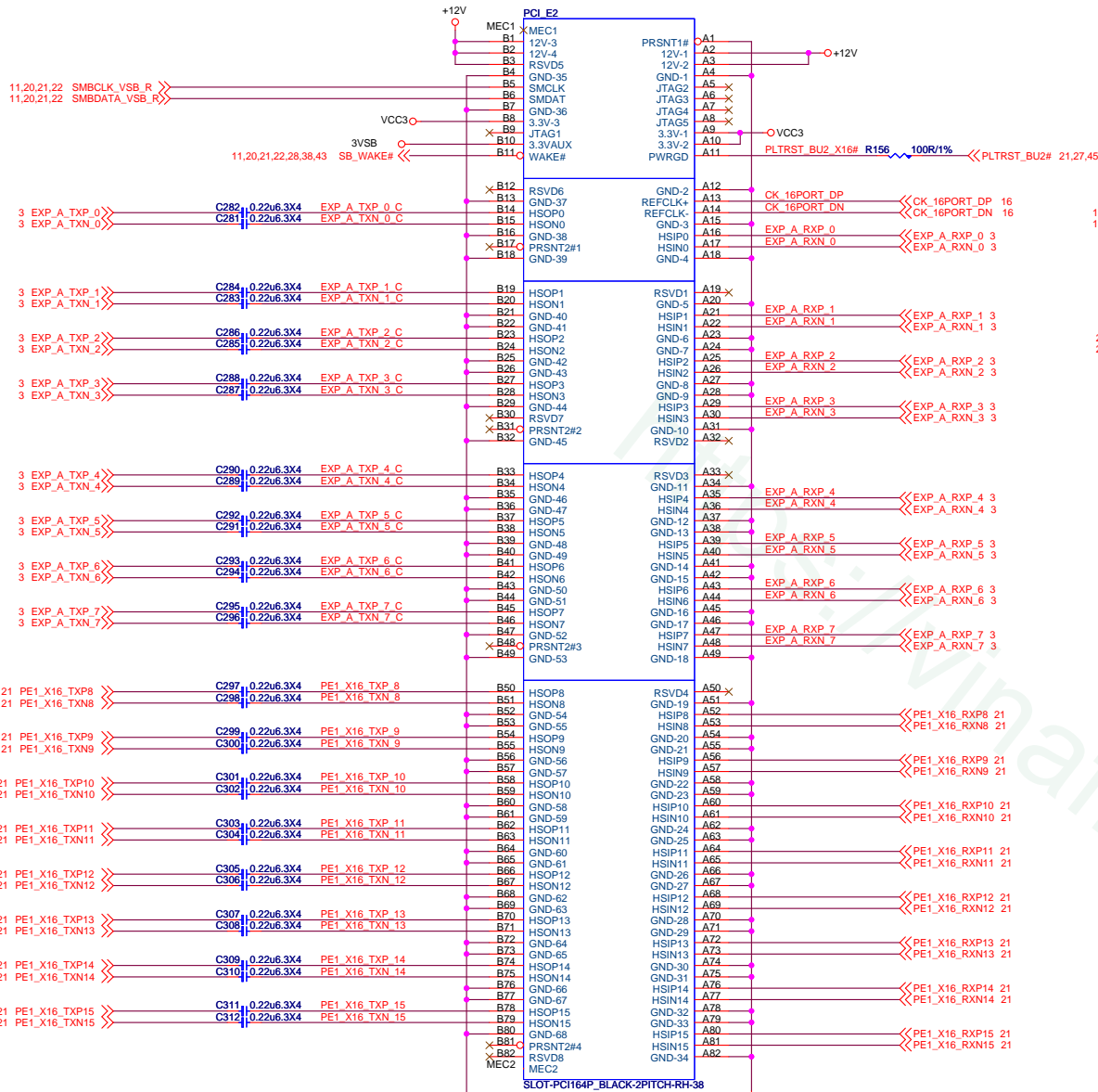


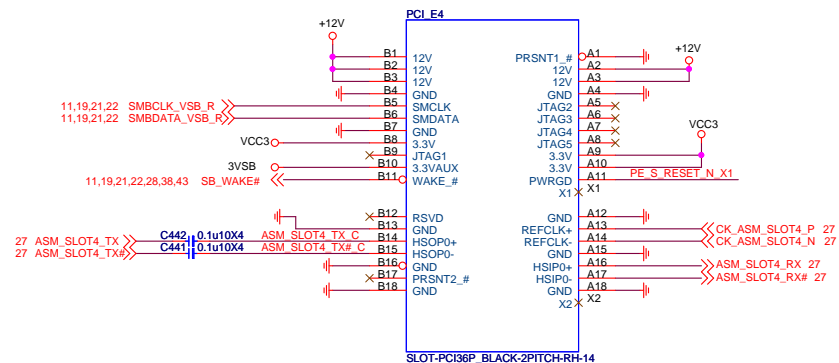
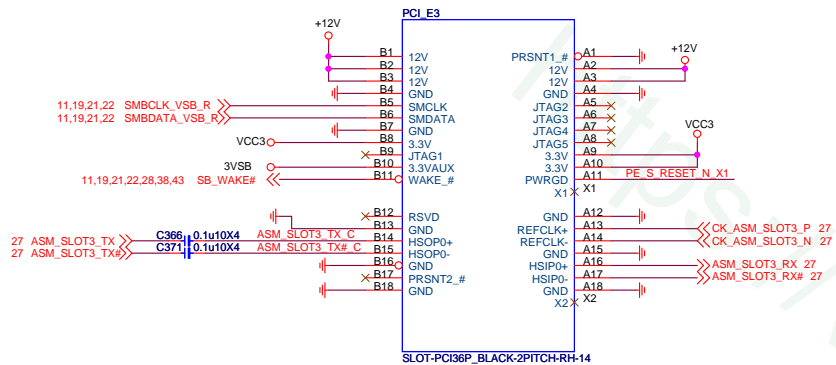
FLASH CONNECTOR



JTAG for SW DEBUG

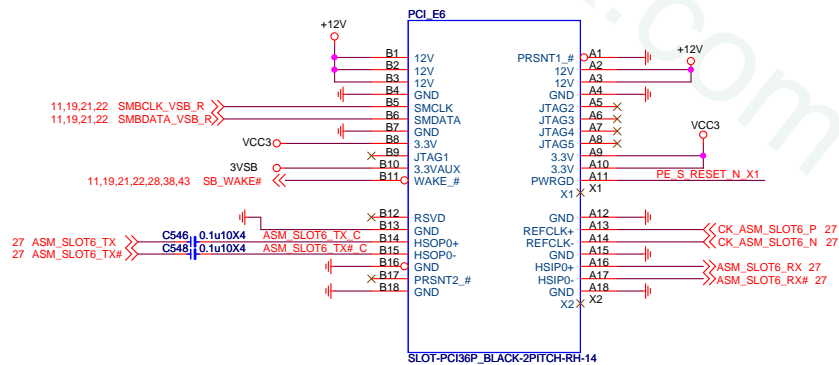




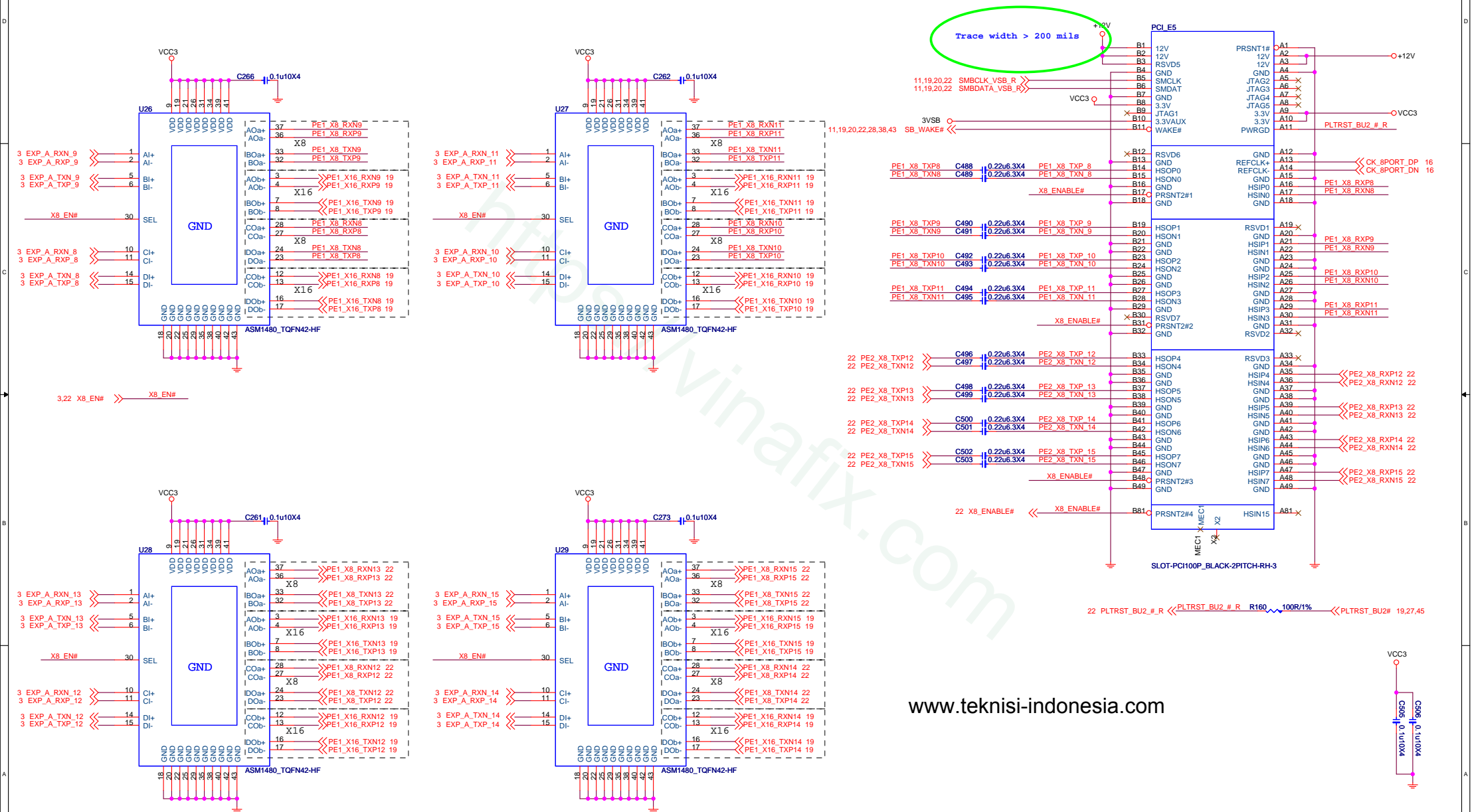


2014.03.12

PE_S_RESET_N X1 R327 100R/1% PE_S_RESET_N_1184 19,27



PCI_Express X8 Slot (Share with PCI_E x16 Slots)



GPIO72

0: BIOS MODE
1: HW MODE

If USE HW MODE (Default)

PCH_GPIO24 & PCH_GPIO28 programming to GPI

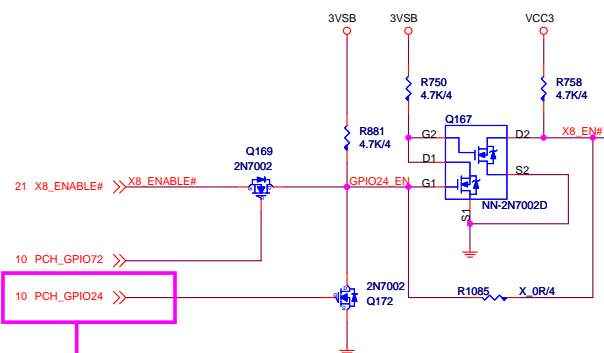
PCH_GPIO72 programming GPO

If USE BIOS MODE

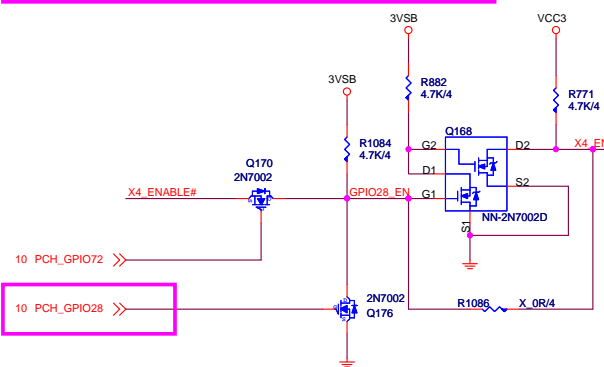
PCH_GPIO24 & PCH_GPIO28 & PCH_GPIO72

programming to GPO

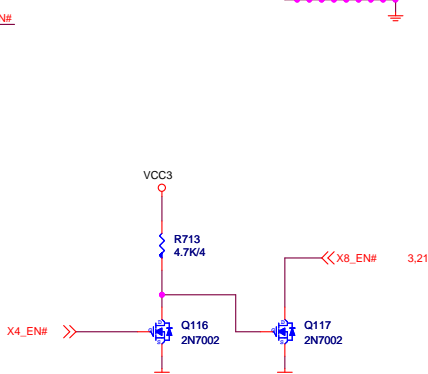
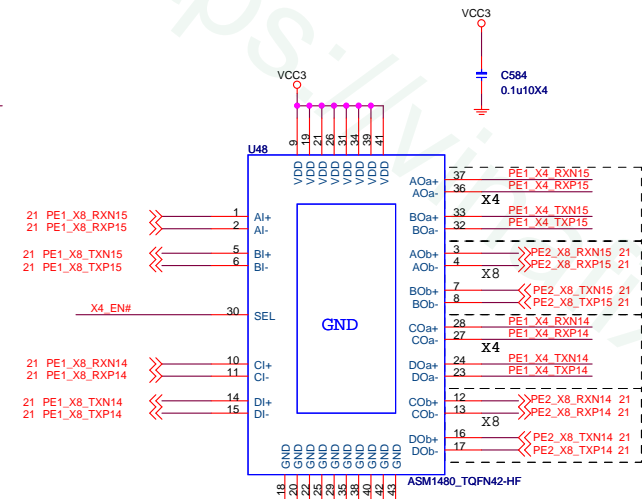
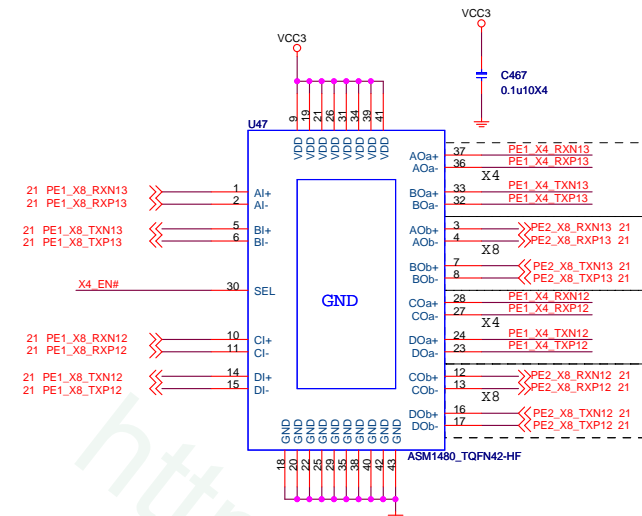
PCH Status	GPIO24	GPIO28	GPIO72
AUTO	GPI	GPI	1
16,0,0	0	0	0
8,8,0	1	0	0
8,4,4	1	1	0



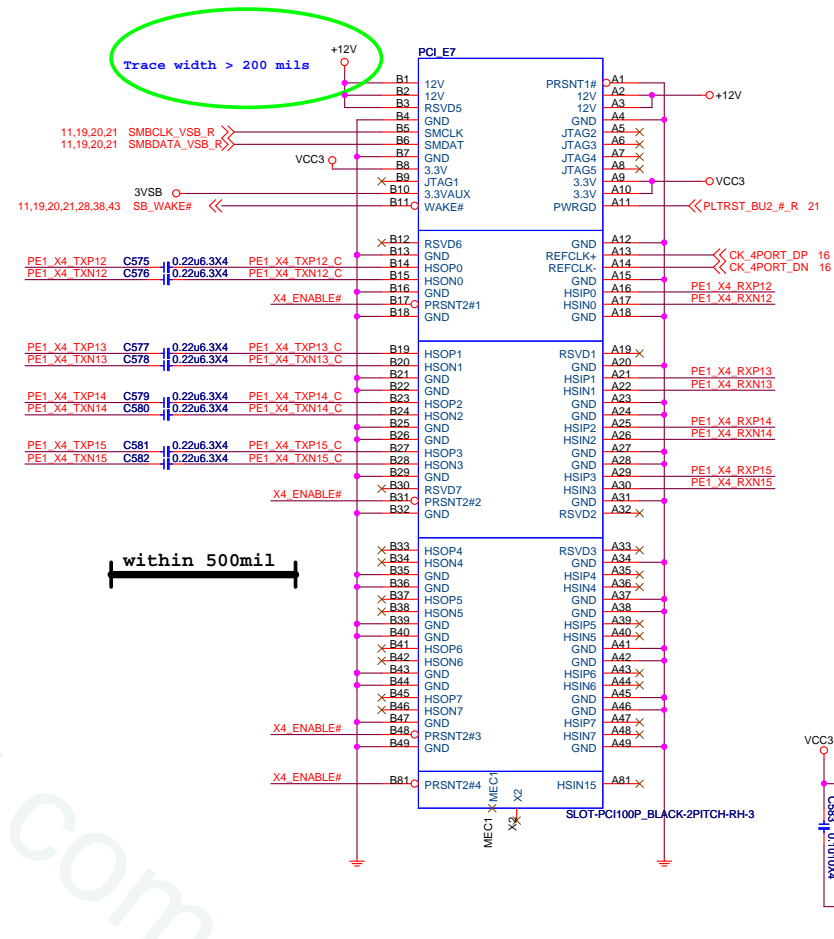
Please choose PCH GPIO default LOW
Patch Clear CMOS PCH GPIO24 default to LOW issue



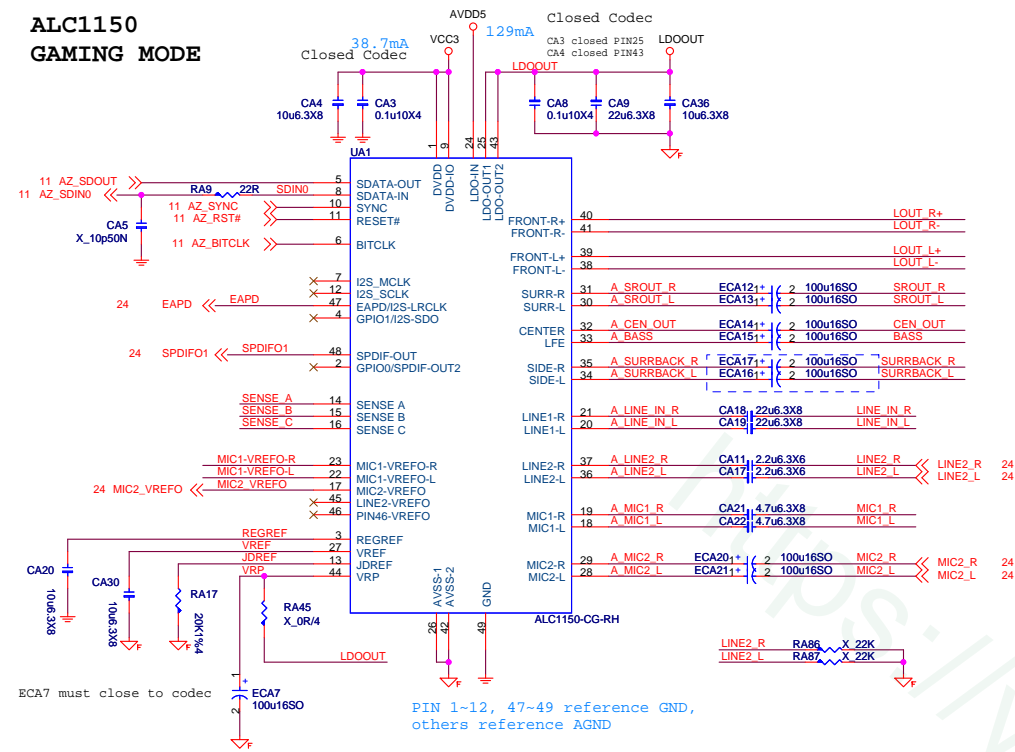
Please choose PCH GPIO default LOW
Patch Clear CMOS PCH GPIO24 default to LOW issue



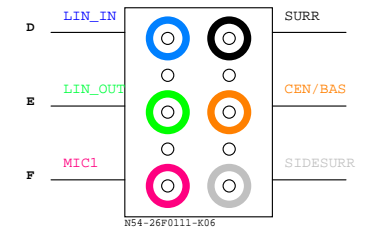
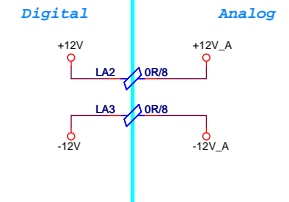
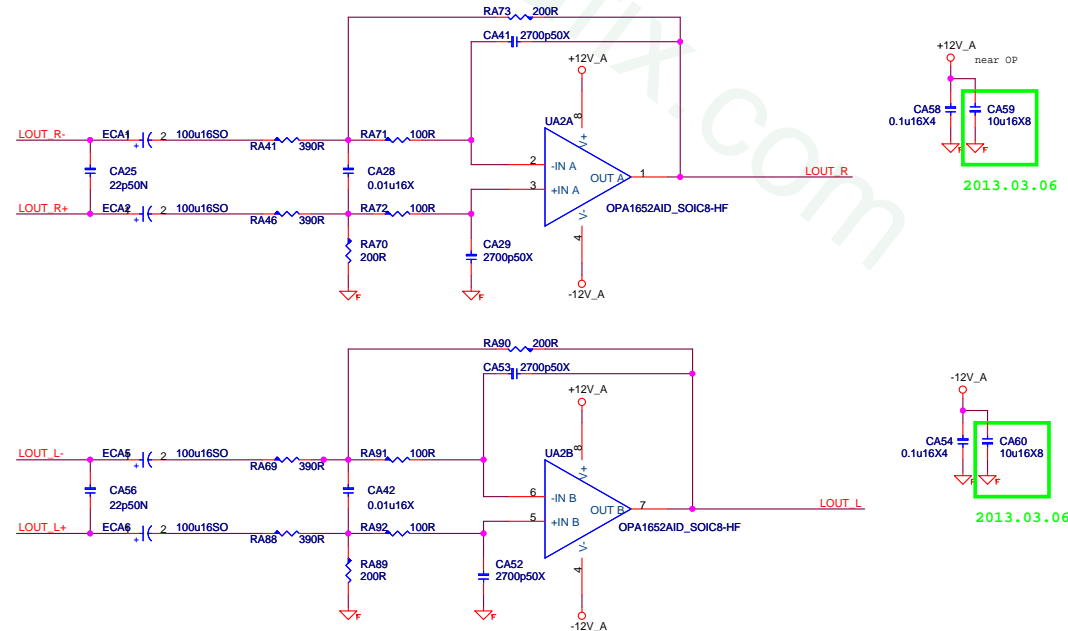
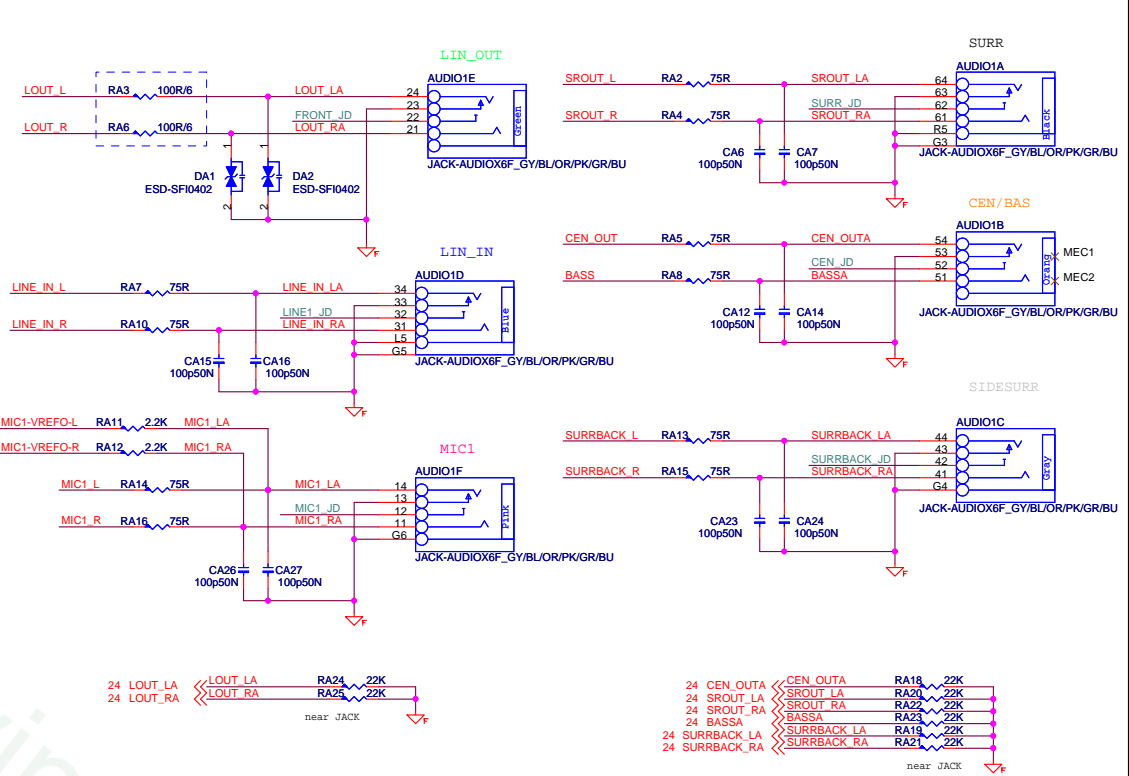
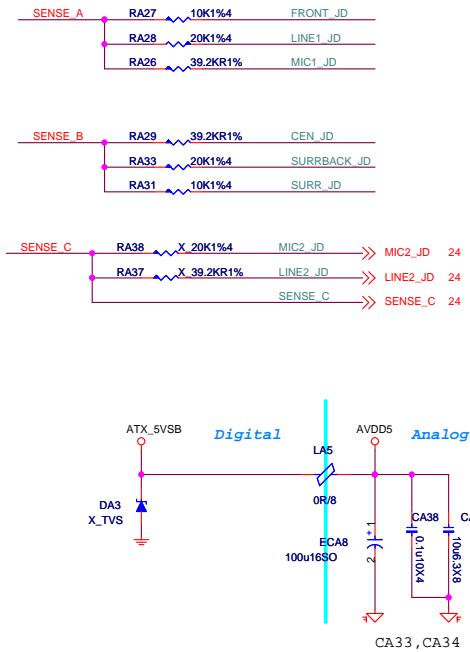
PCI_Express X4 Slot(by CPU)

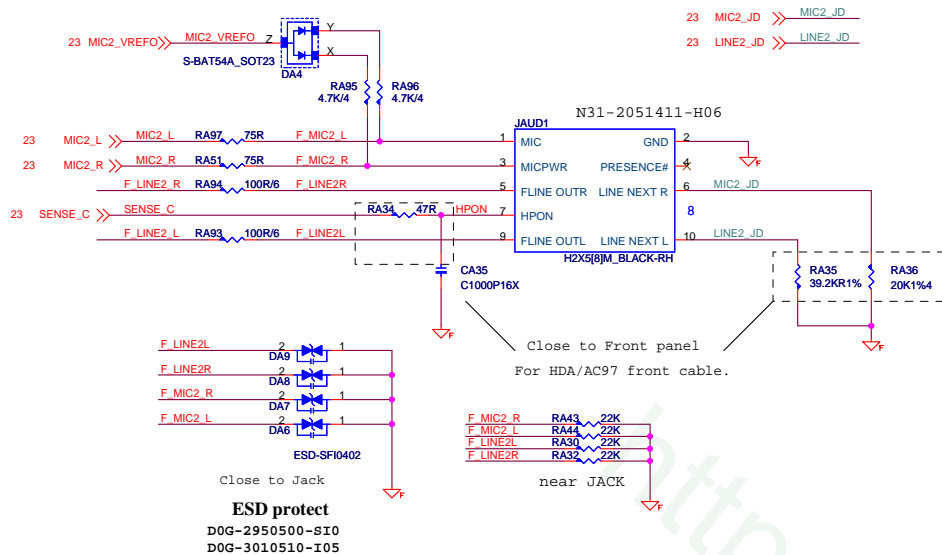


ALC1150
GAMING MODE

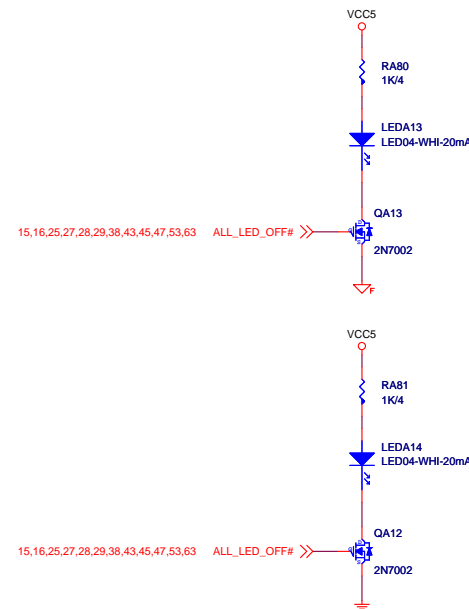


Closed Codec



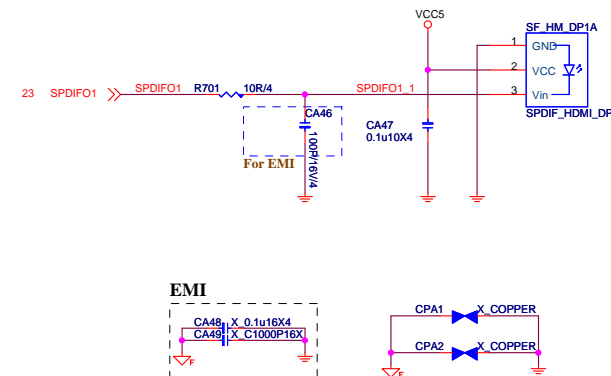


AUDIO LED



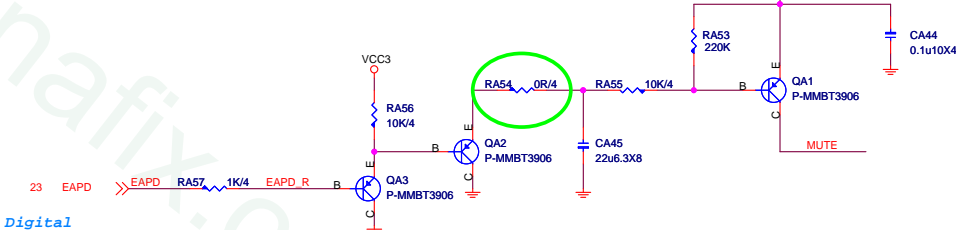
SPDIF OUT

N58-42M0021-F02 (HDMI+DP+SPDIF)
N58-06F0201-K06



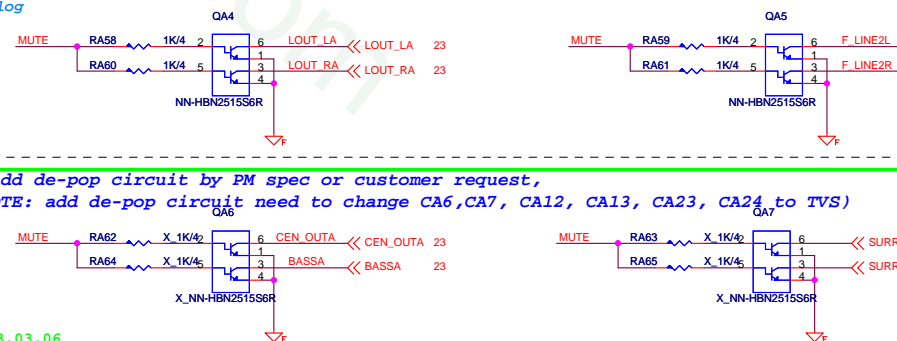
Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)

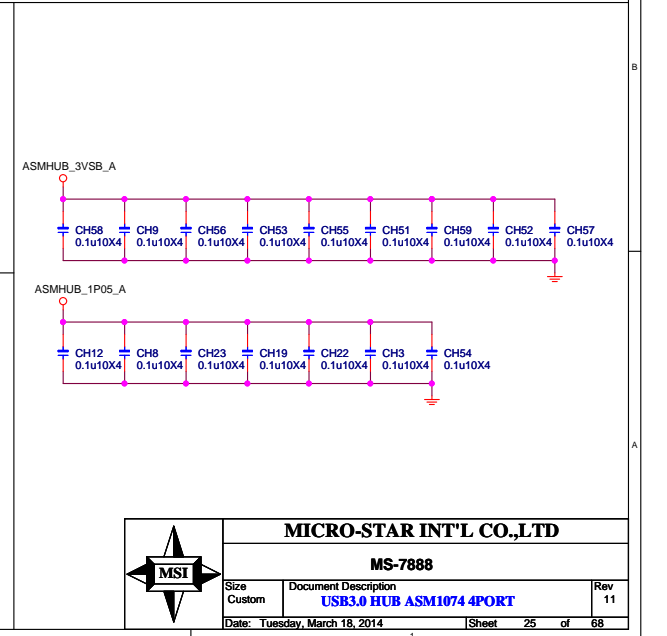
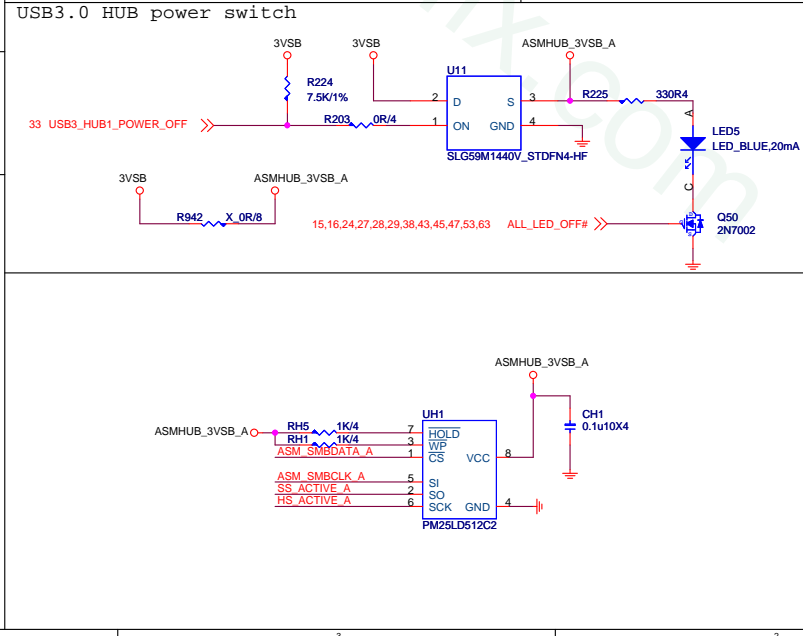
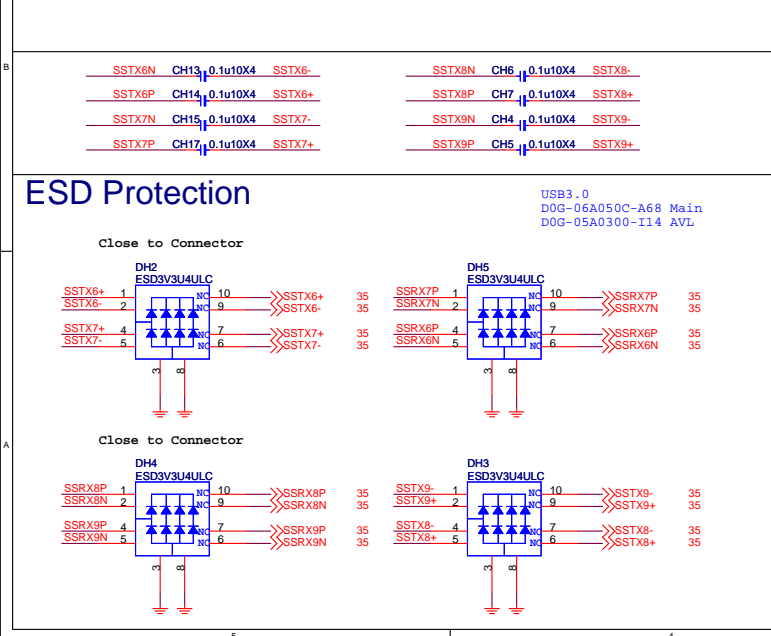
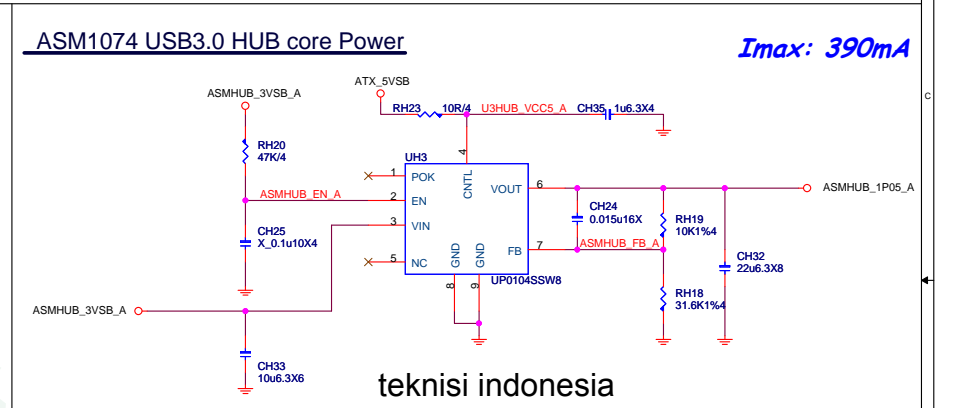
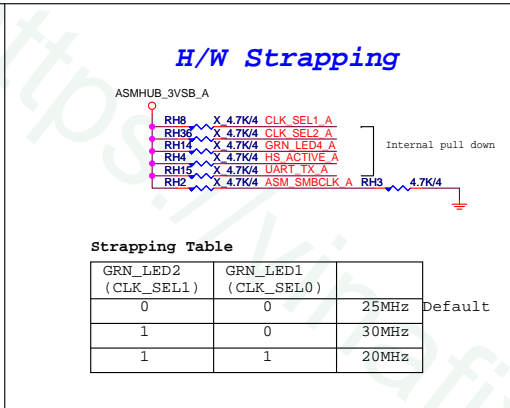
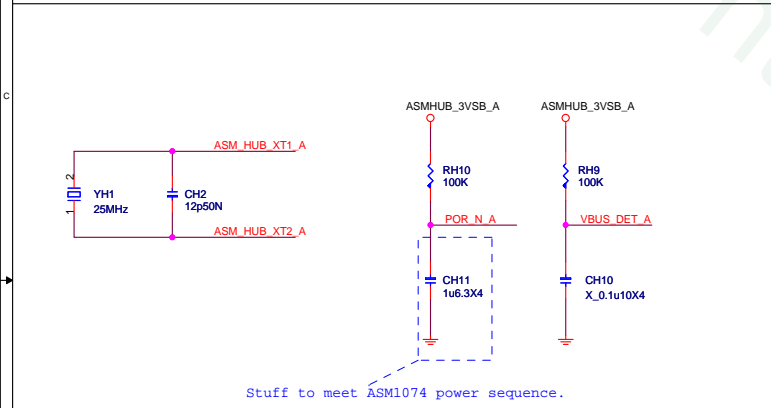
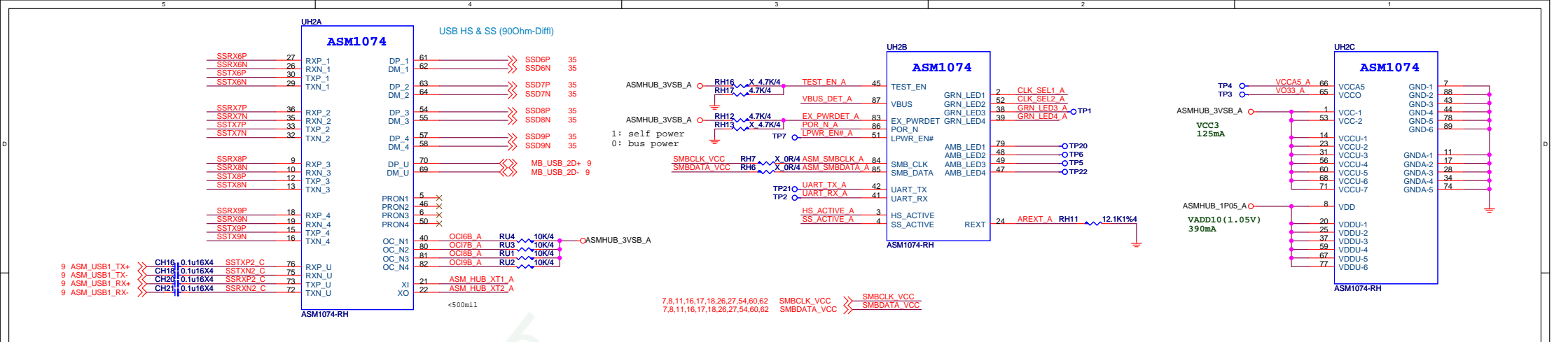
2013.03.06

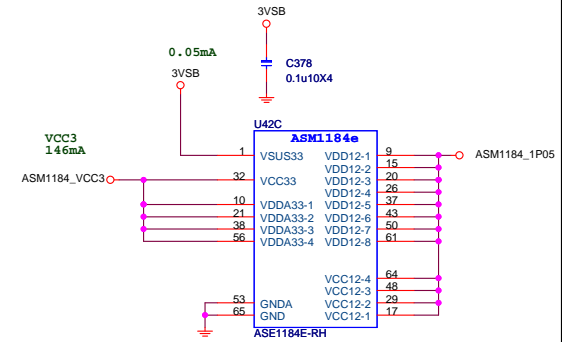
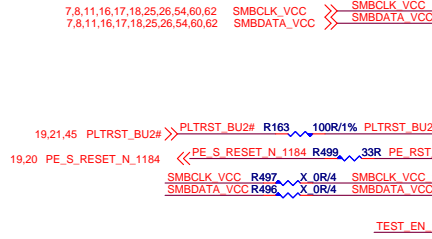
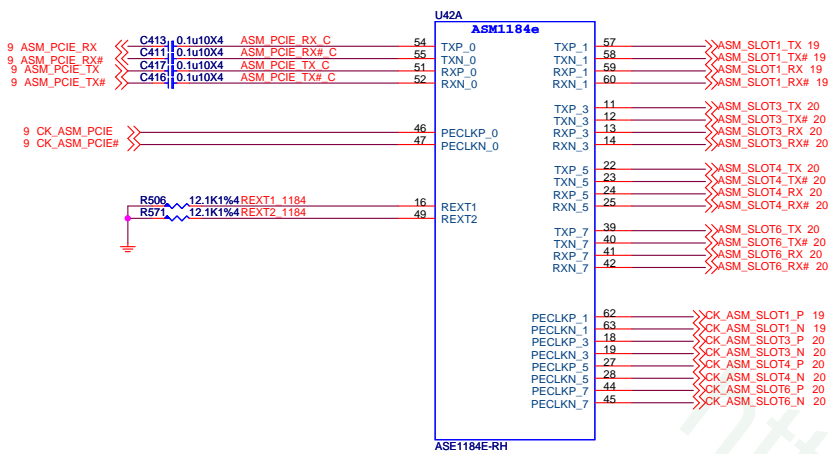


MICRO-STAR INT'L CO.,LTD

MS-7888

Size	Document Description	Rev
Custom	AUDIO ALC1150	11
Date: Tuesday, March 18, 2014	Sheet 24 of 68	



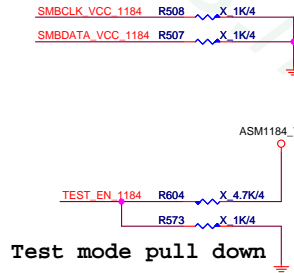
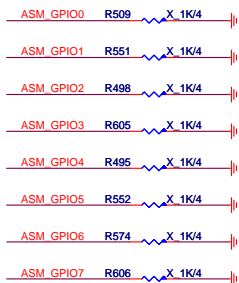


GPIO0	0:PLL mode; 1: bypass mode
GPIO1	clock buffer termination 0: disable ; 1: enable
GPIO2	Reserved for test mode
GPIO3	Reserved for ASM1184e
GPIO4	SMBus enable
GPIO5	SMBus address[0]
GPIO6	SMBus address[1]
GPIO7	SMBus address[2]
MSCL	I2C enable

GPIO4	MSCL	Function
0	0	(MSCL,MSDA) is no function
0	1	(MSCL,MSDA) is I2C,chip is master
1	0	(MSCL,MSDA) is SMBus, chip is salve
1	1	(MSCL,MSDA) is SMBus, chip is salve

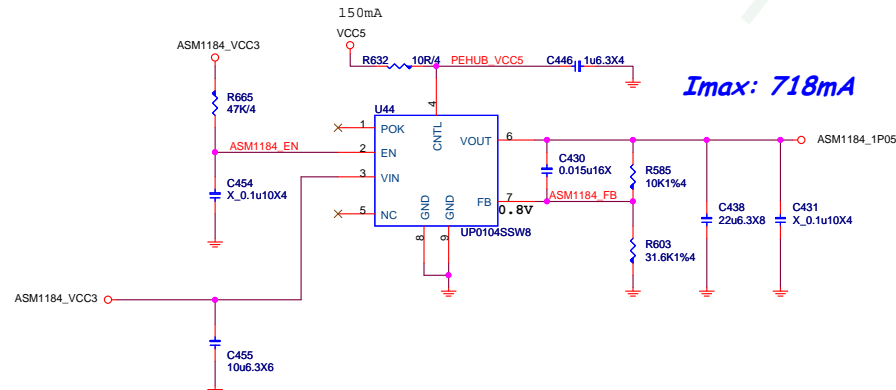
H/W Strapping

Internal pull high 50Kohm

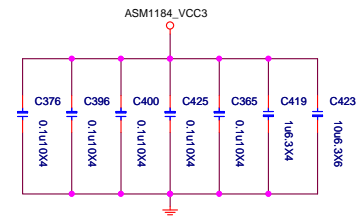
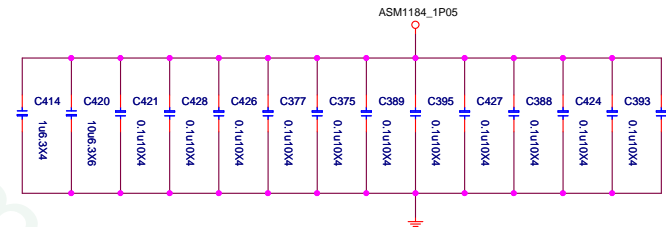
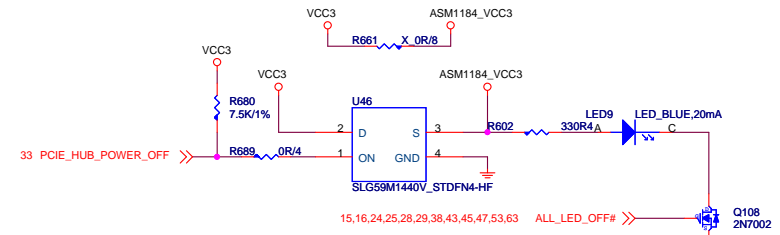


Test mode pull down

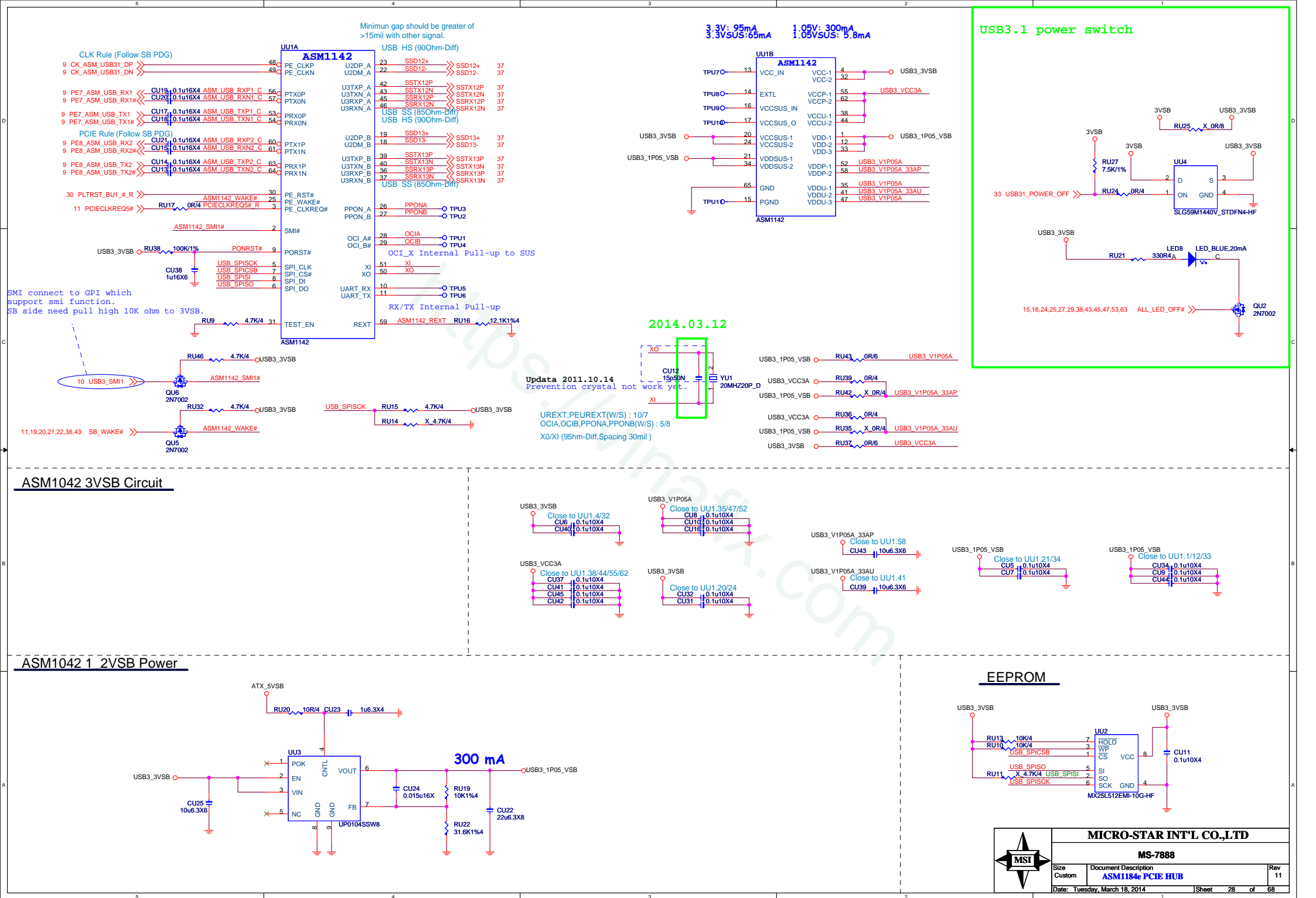
ASM1184 PCIE HUB core Power



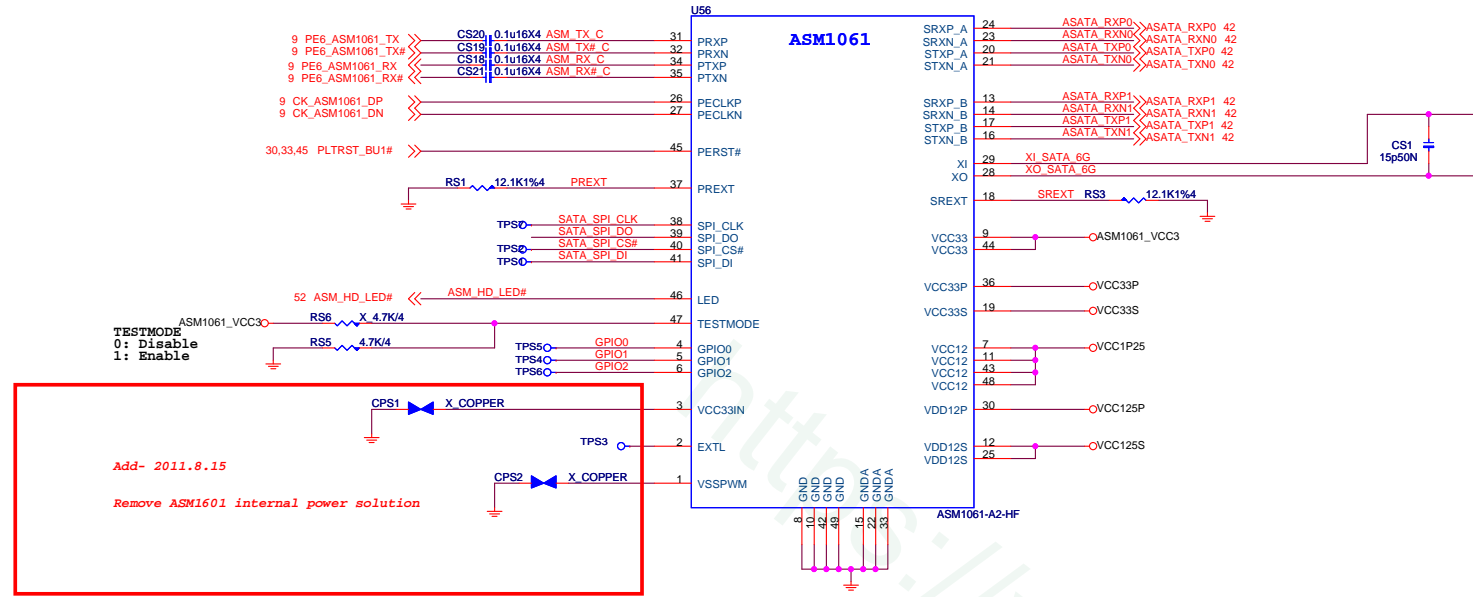
PCIE HUB power switch



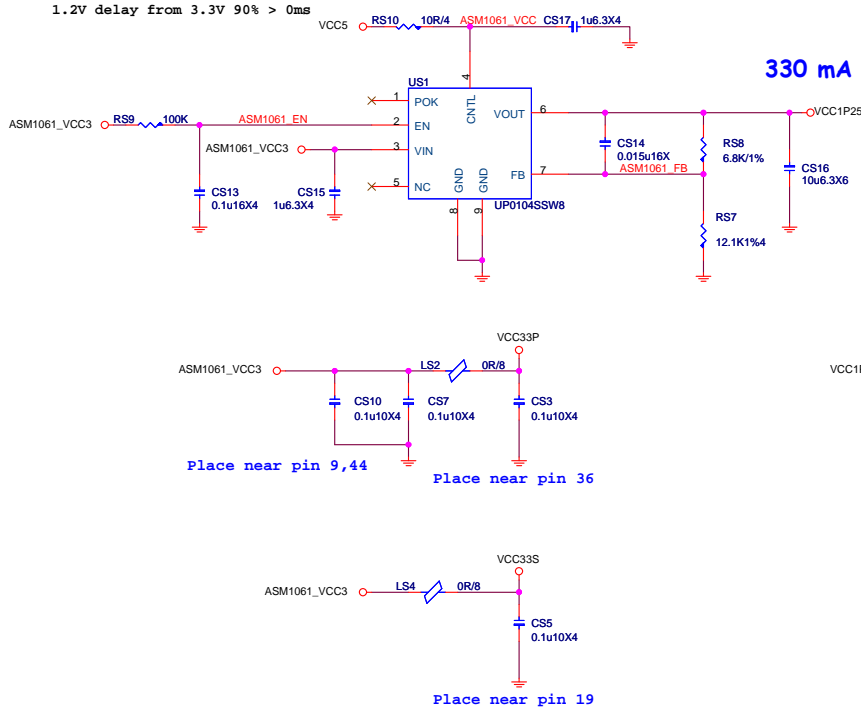
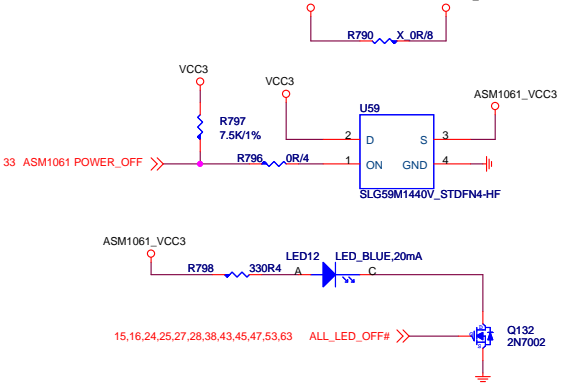
MICRO-STAR INT'L CO.,LTD			
MS-7888			
Size	Document Description	Rev	
Custom	ASM1184e PCIE HUB	11	
Date: Tuesday, March 18, 2014		Sheet	27 of 68



ASM1061 SATA6G

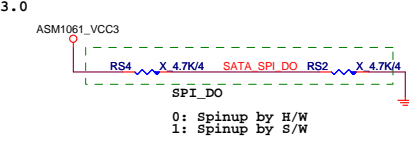


ASM1061 power switch



ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

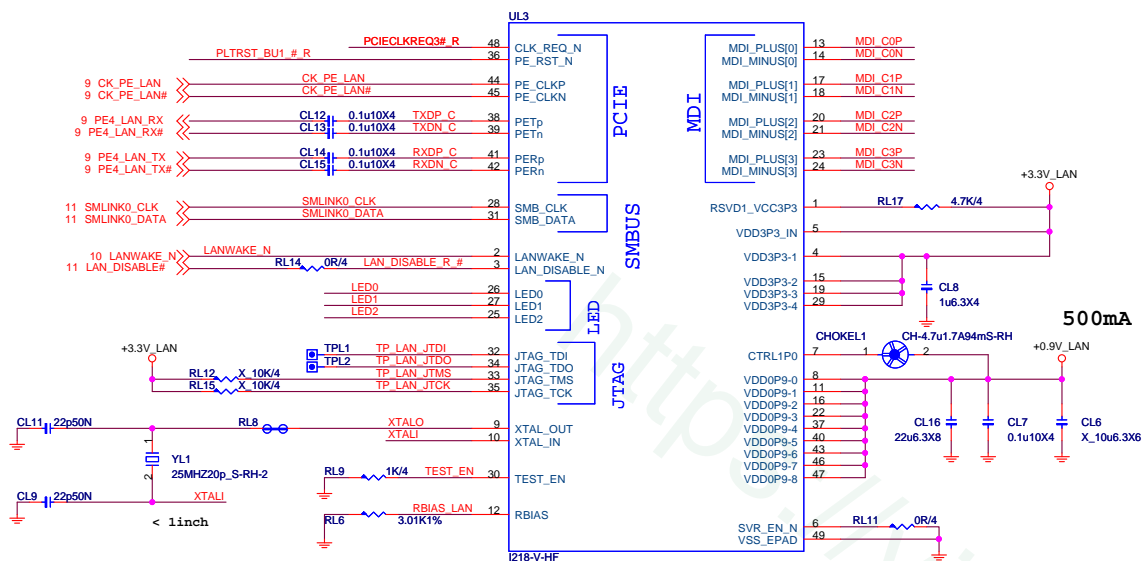


Add- 2011.3.18
SATA_SPI_DO don't need pull up (integrated pull-up)
or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

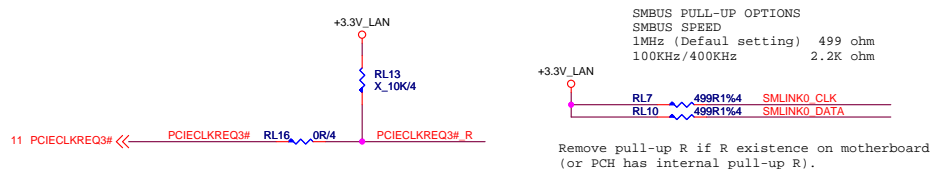
Intel Clvrkville I218V PHY

2014.03.12

29,33,45 PLTRST_BU1# >> R136 100R/1% PLTRST_BU1#_R >> PLTRST_BU1#_R 28

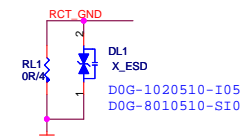
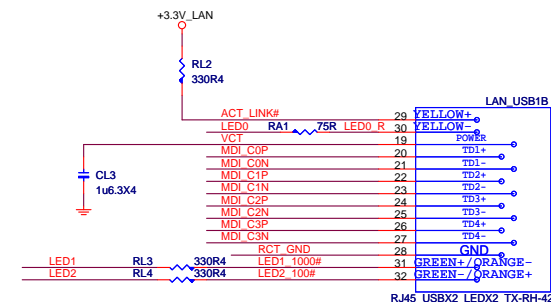
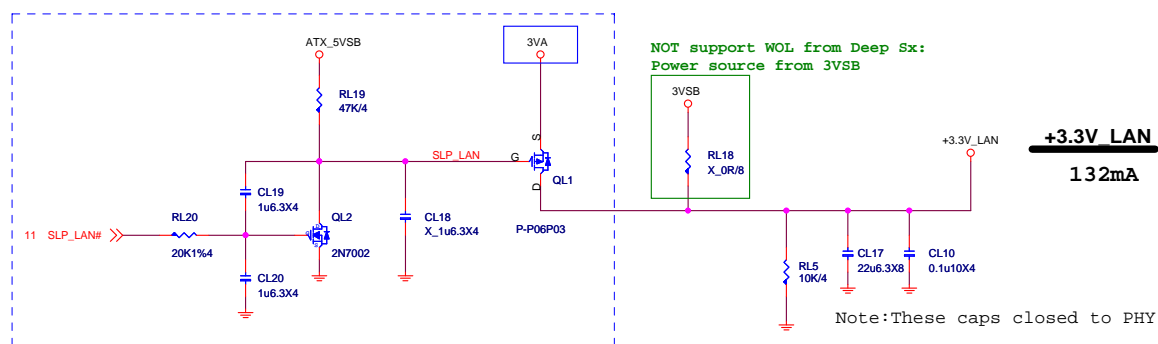


PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is left as NC

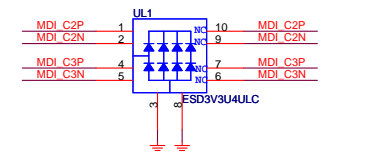
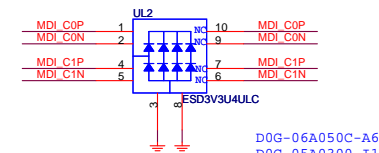
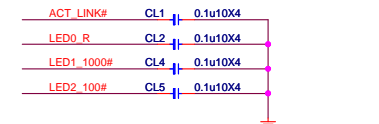


The 10Kohm pull-up resistor of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.


support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218.

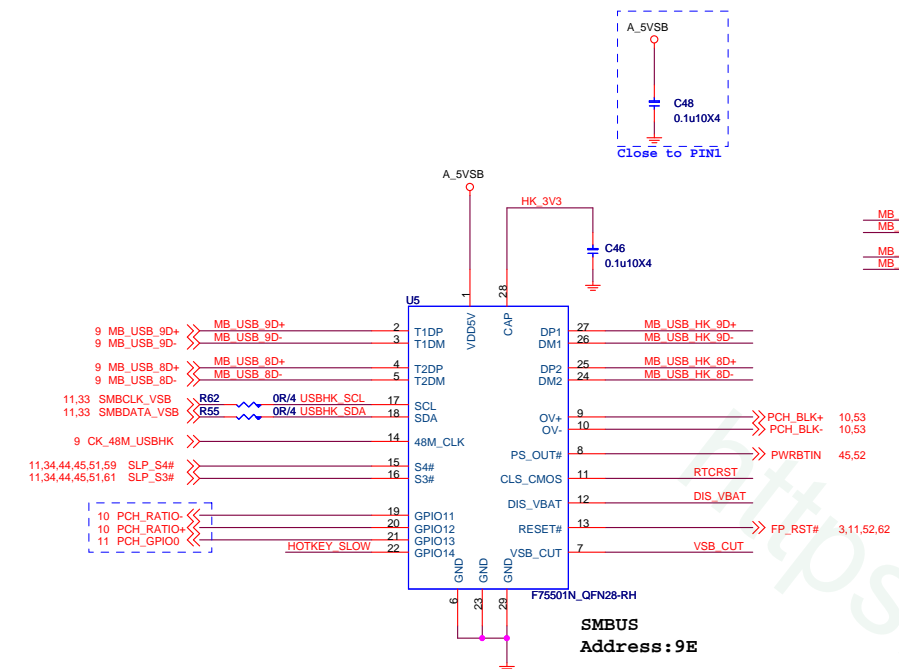


For EMI



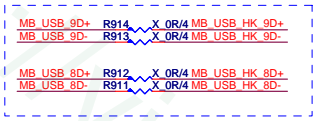
Do not pair MDI0 and MDI1 on the same TVS device
(avoid LAN POE connecting issue).
Other pairing combination is ok.

	MICRO-STAR INT'L CO.,LTD		
	MS-7888		
	Size	Document Description	Rev
	Custom	LAN - Intel LANI218V	11
	Date: Tuesday, March 18, 2014		Sheet 30 of 68

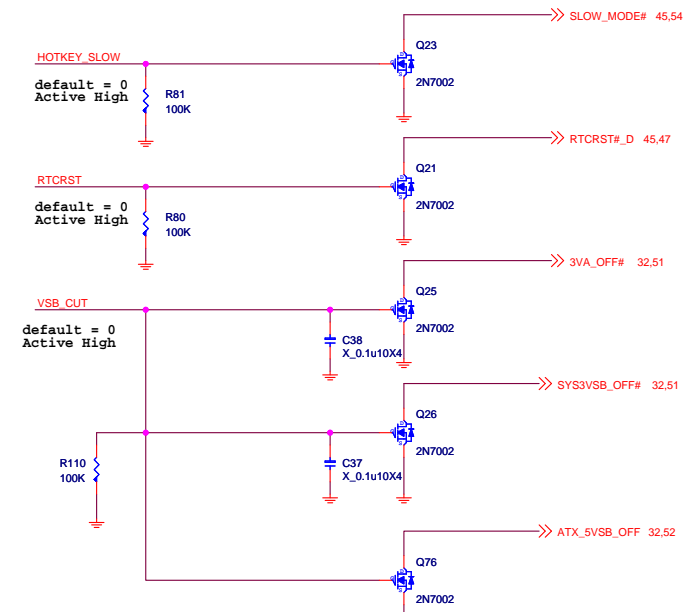


ESD close to connector.
(use usb3.0 ESD for eye diagram)

F75501 OV+(PIN9) Connection to PCH GPIO3
F75501 OV-(PIN10) Connection to PCH GPIO2
(to SIO PSIN PIN)

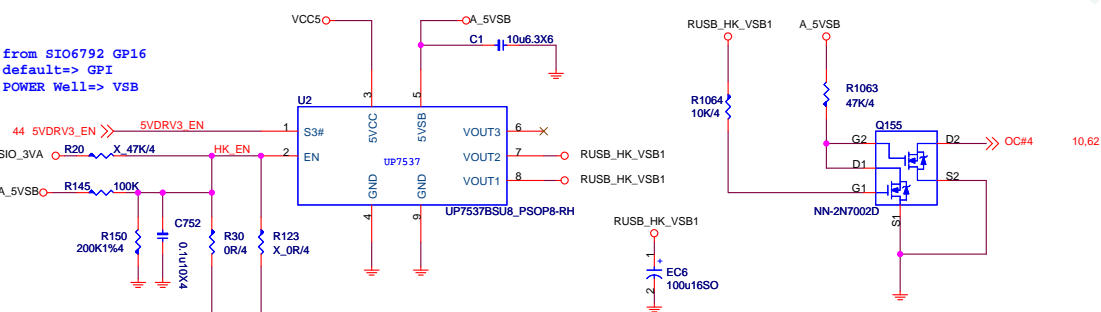


Co-lay by option.
For PM spec request.

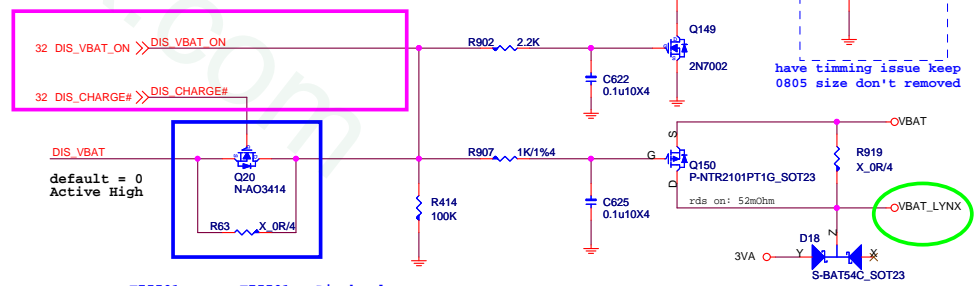
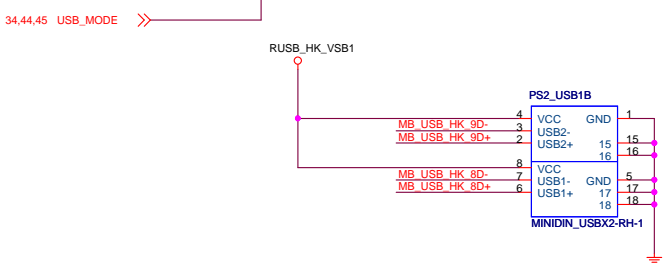


F75501 GPIO11 Connection to PCH GPIO4
F75501 GPIO12 Connection to PCH GPIO5
F75501 GPIO13 Connection to PCH GPIO1
(OD,default=High,Active Low)

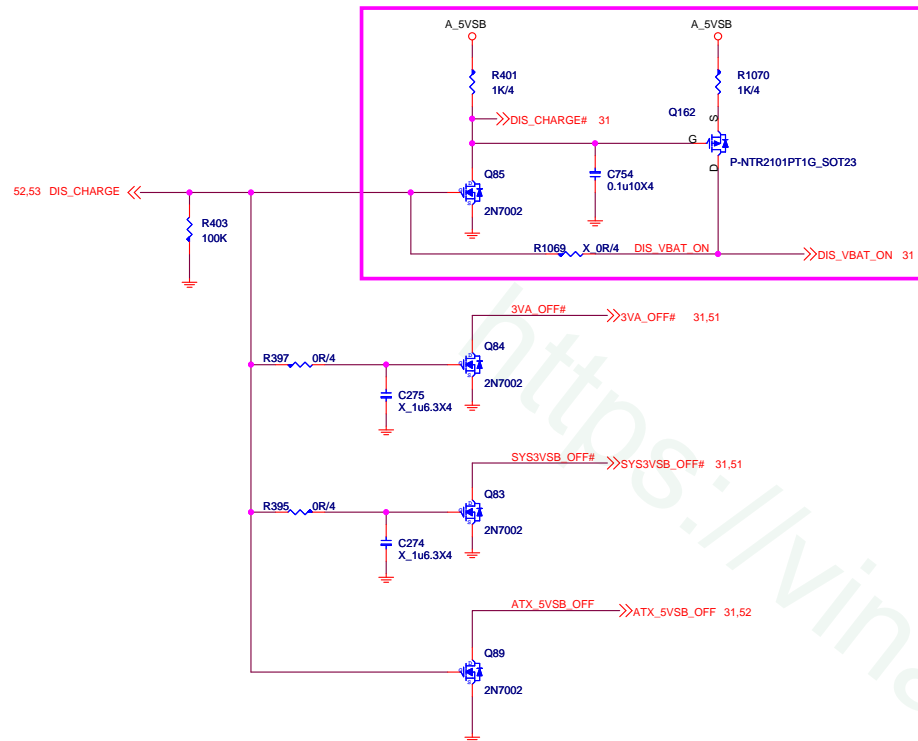
All PCH GPI need smi function and default=GPI or Native.



REAR USB PORT 8,9 (With PS2)



F75501 only , F75501 + Pin header
Mos X O X
R X O X




MICRO-STAR INT'L CO.,LTD

MS-7888

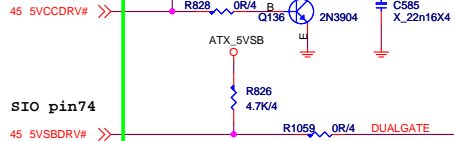
Size Custom	Document Description Discharge	Rev 11
Date: Tuesday, March 18, 2014	Sheet 32 of 68	



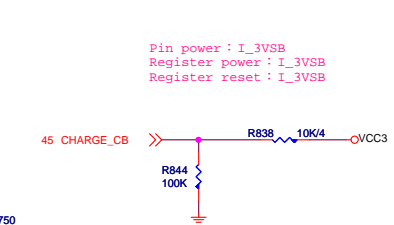
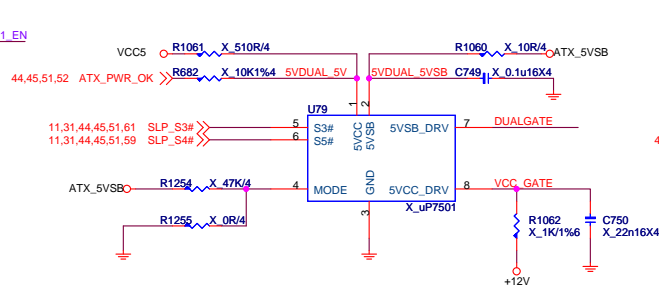
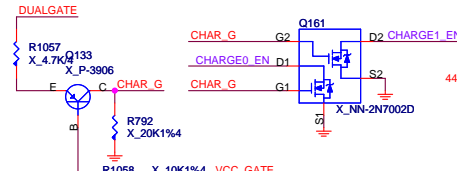
	MICRO-STAR INT'L CO.,LTD		
	MS-7888		
	Size Custom	Document Description TPM/GPIO controller	Rev 11
	Date: Tuesday, March 18, 2014		Sheet 33 of 68

5VDUAL_USB

6792 SIO pin71

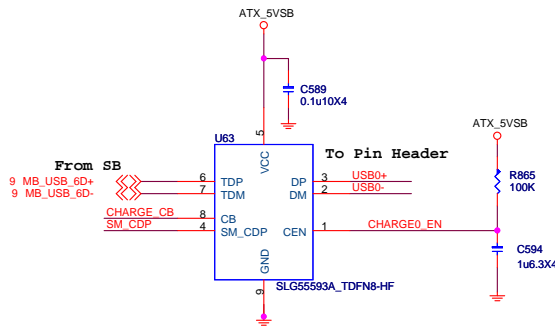
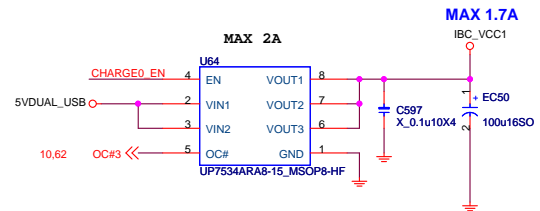


6792 SIO pin74

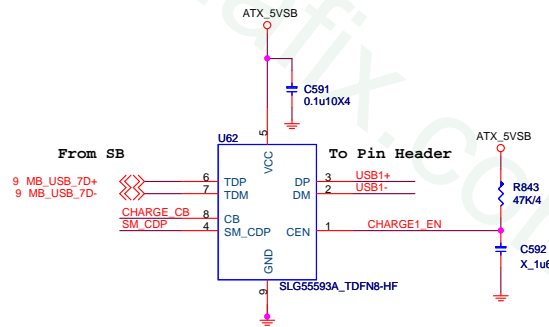
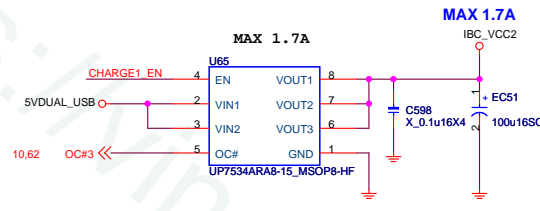


Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB

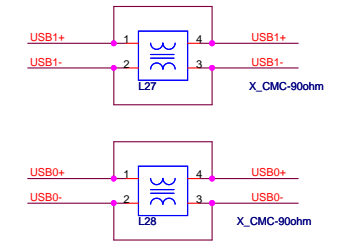
USB POWER PORT 0 For USB Charging



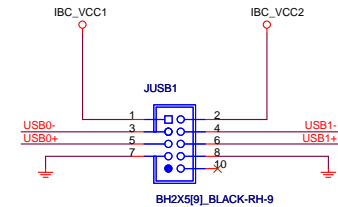
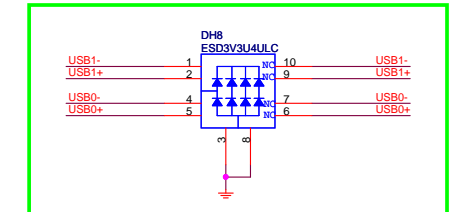
USB POWER PORT 1 For USB Charging



FRONT USB PORT 0,1

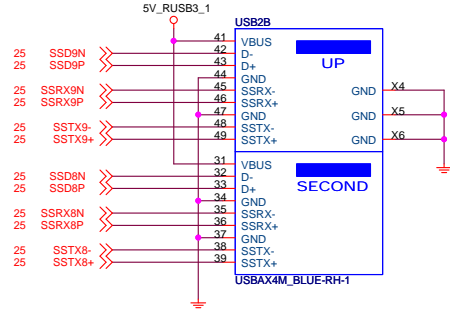
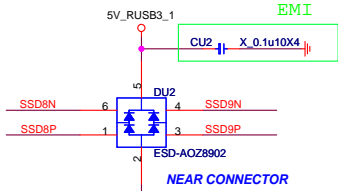
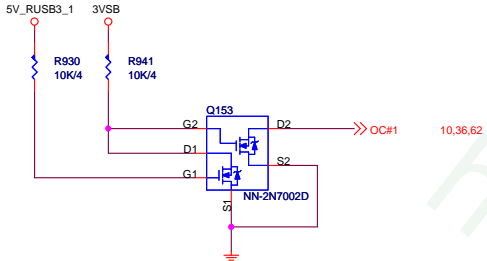


2013.03.06

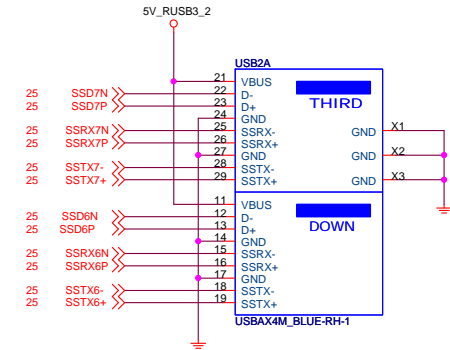
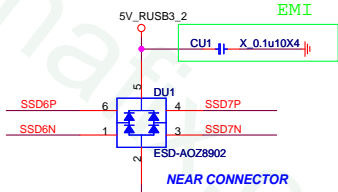
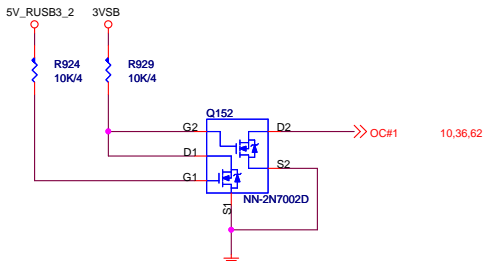


MICRO-STAR INT'L CO.,LTD			
MS-7888			
Size	Custom	Document Description	Rev
		USB CHARGE_SLG55593A	11
Date:	Tuesday, March 18, 2014	Sheet	34 of 68

Rear I/O



Rear I/O

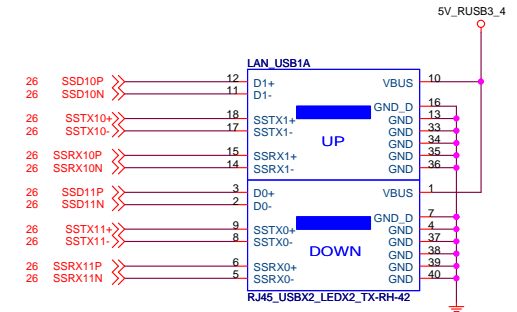
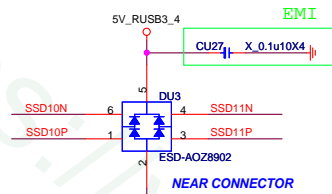
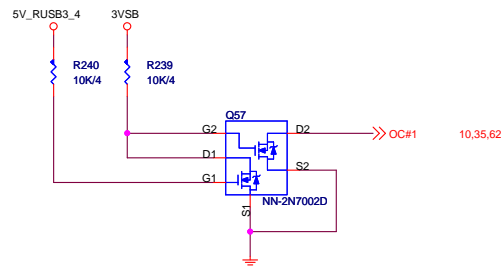


MICRO-STAR INT'L CO.,LTD

MS-7888

Size Custom	Document Description ASM1074 USB3.0 CON 4Port 5~8	Rev 11
Date: Tuesday, March 18, 2014		Sheet 35 of 68

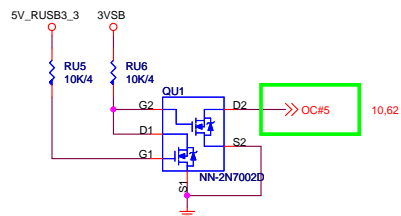
Rear I/O



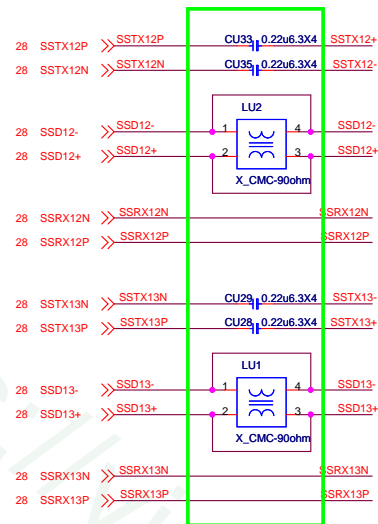
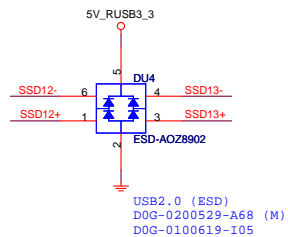
MICRO-STAR INT'L CO.,LTD

MS-7888

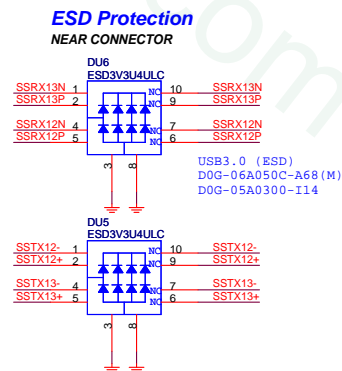
Size	Document Description	Rev
Custom	ASM1074 USB3.0 CON 4Port 1-4	11
Date:	Tuesday, March 18, 2014	Sheet 36 of 68



OC# signal connect to
SB OC pin.

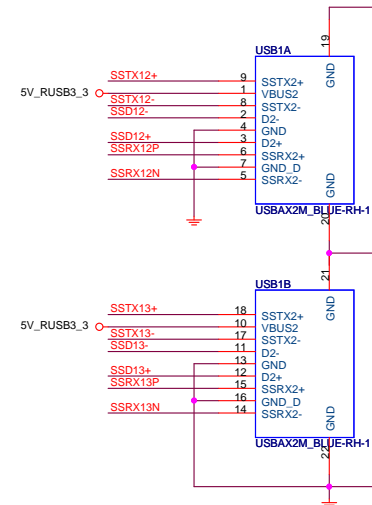


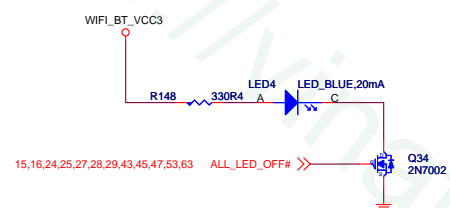
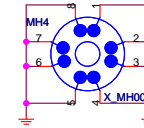
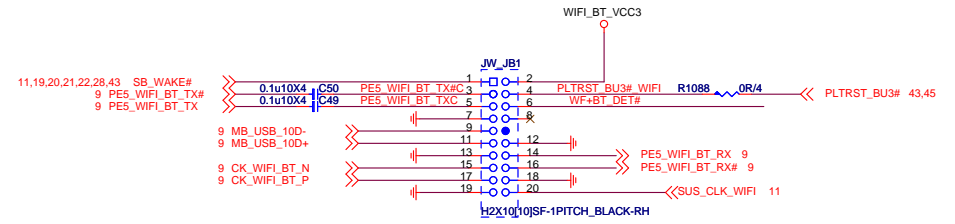
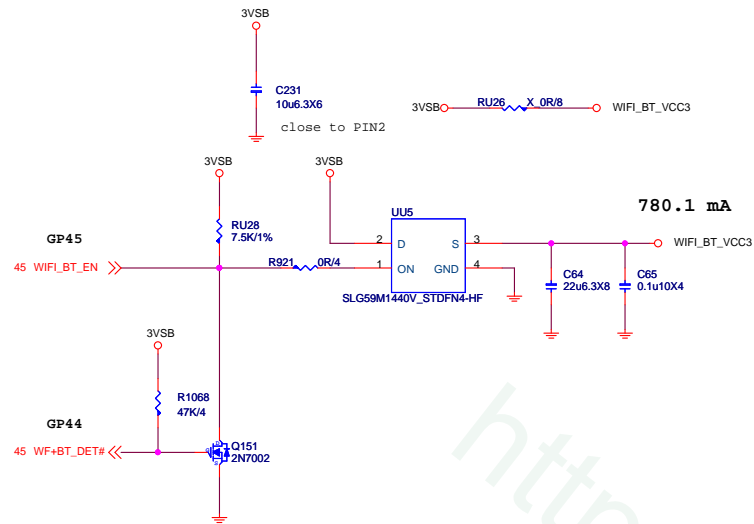
若Layout空間不足可不預留此部分choke

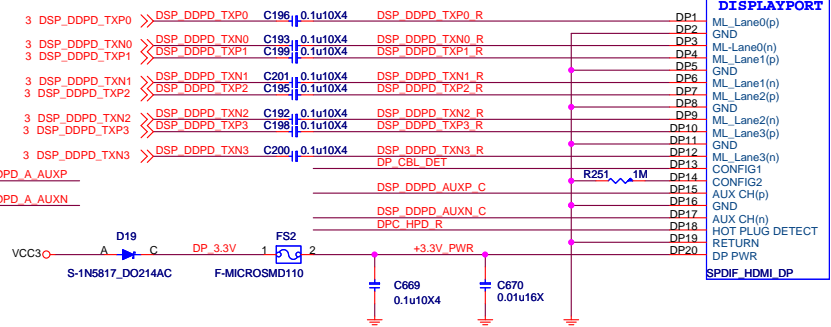
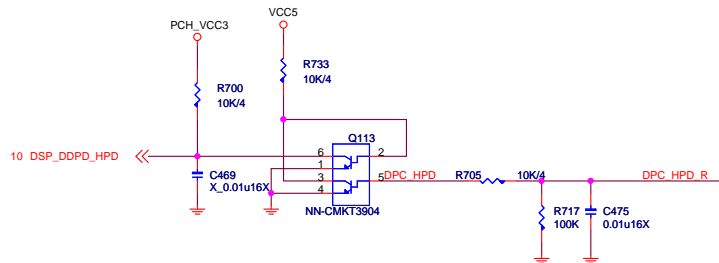
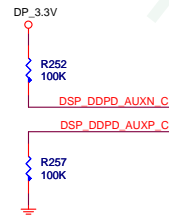
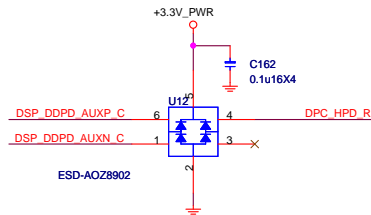
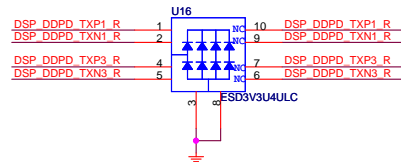
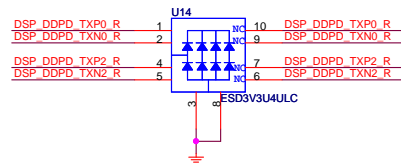


Rear USB3 CONN

Important---
If USB3.0 signal connect to front pin header,
please must less than 0.6 inch, short trace
has better eye diagram with some bad fly cable by SI customer.

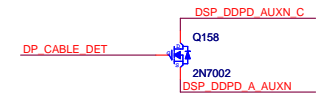
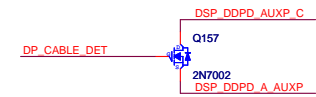




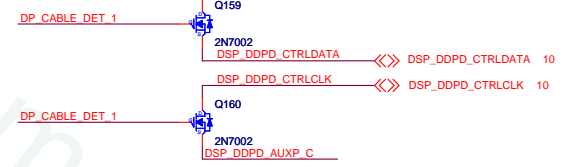


SF_HM_DP1C	
DISPLAYPORT	
DP1	ML_Lane0(p)
DP2	GND
DP3	ML_Lane0(n)
DP4	ML_Lane1(p)
DP5	GND
DP6	ML_Lane1(n)
DP7	ML_Lane2(p)
DP8	GND
DP9	ML_Lane2(n)
DP10	ML_Lane3(p)
DP11	GND
DP12	ML_Lane3(n)
DP13	CONFIG1
DP14	CONFIG2
DP15	AUX_CH(p)
DP16	GND
DP17	AUX_CH(n)
DP18	HOT PLUG DETECT
DP19	RETURN
DP20	DP_PWR
SPDIF HDMI_DP	

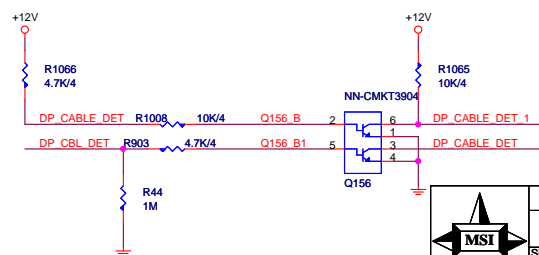
DisplayPort*Interoperability Implementation



PS:DSP_DDPD_CTRLCLK
PULL HIGH 3.3V 2.2K ohm on chip side



PS:DSP_DDPD_CTRLDATA
PULL HIGH 3.3V 2.2K ohm on chip side



MICRO-STAR INT'L CO.,LTD		
MS-7888		
Size	Document Description	Rev
Custom	Display port connector	11
Date:	Tuesday, March 18, 2014	Sheet 39 of 68

HDMI level shifter

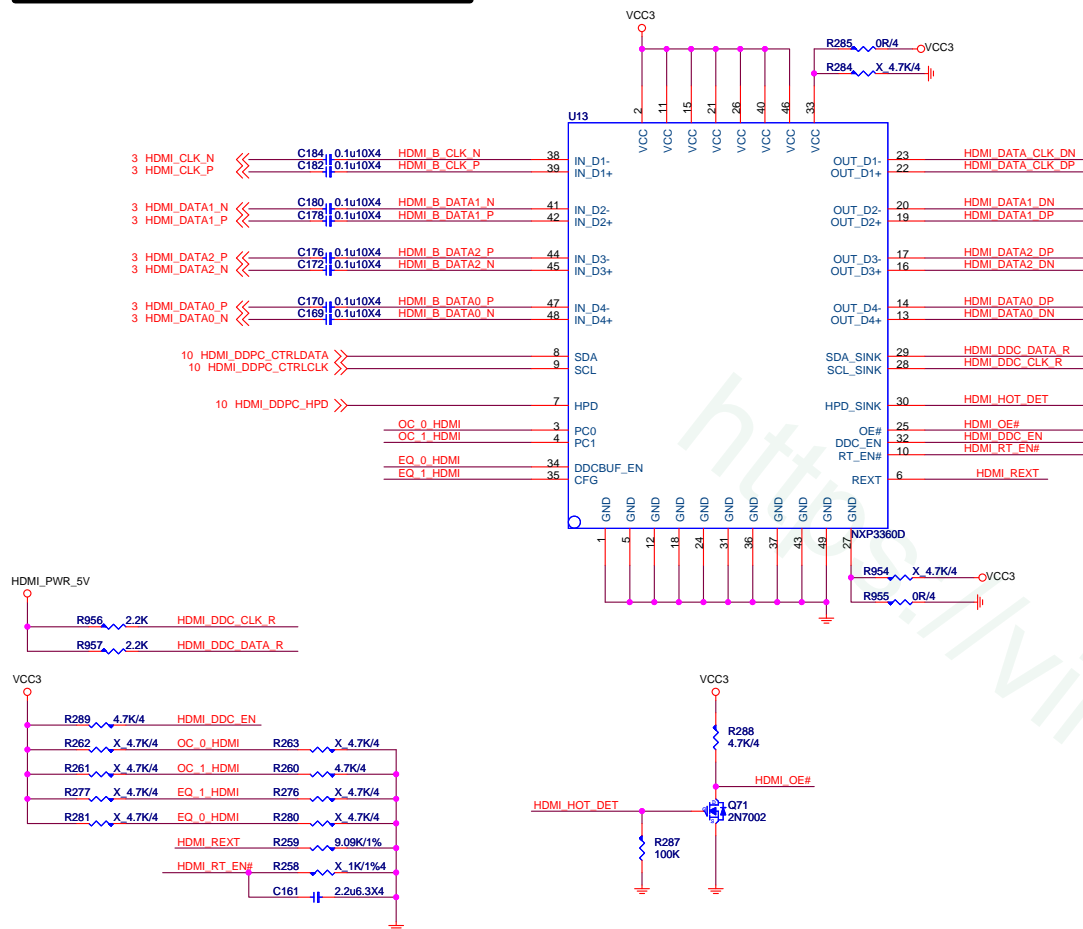
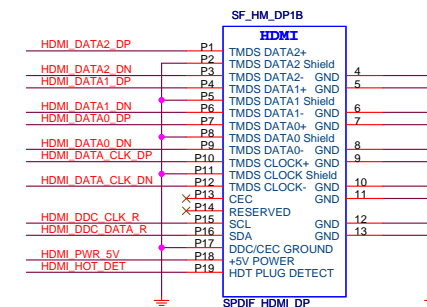


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

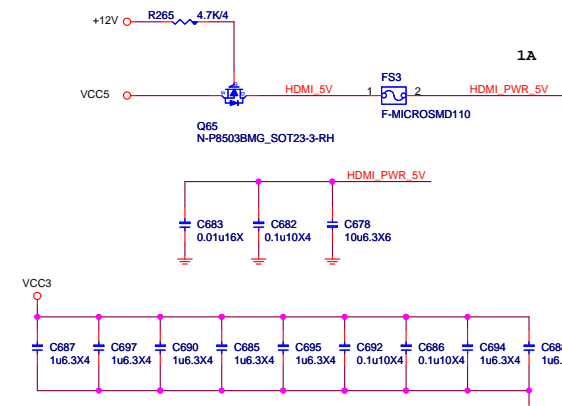
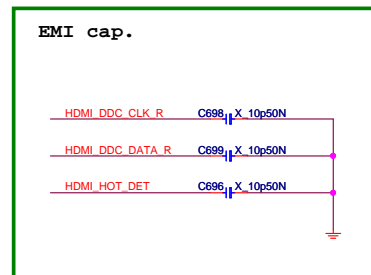
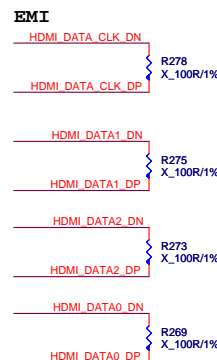
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPDI	DDSP_B_HPDI	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_CTRL_DATA	



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPDI_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

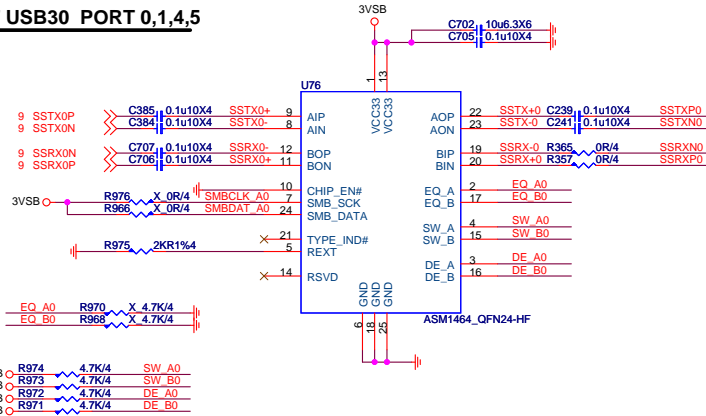
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

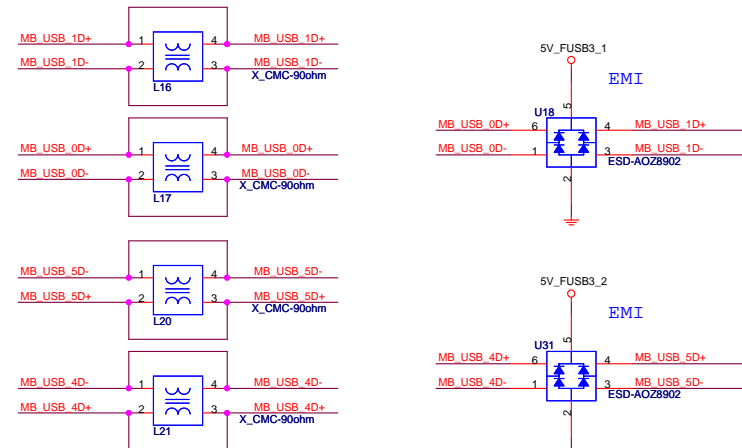
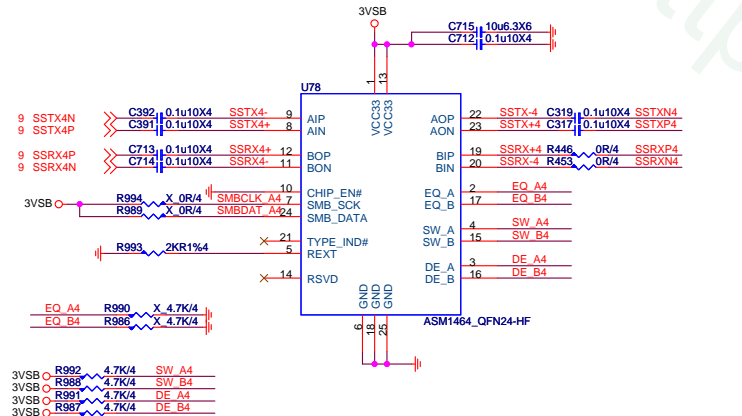


MICRO-STAR INT'L CO.,LTD			
MS-7888			
Size	Document Description	Rev	
Custom	HDMI port connector	11	
Date: Tuesday, March 18, 2014		Sheet	40 of 68

FRONT USB30 PORT 0,1,4,5

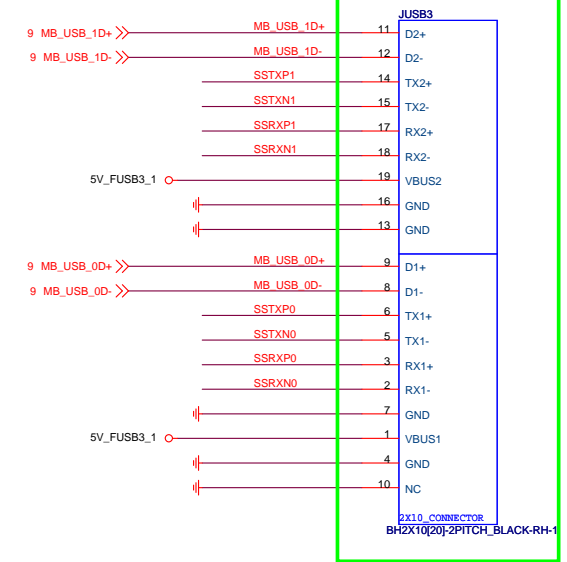


USB3.0: PCH to Re-driver IC Length < 6"



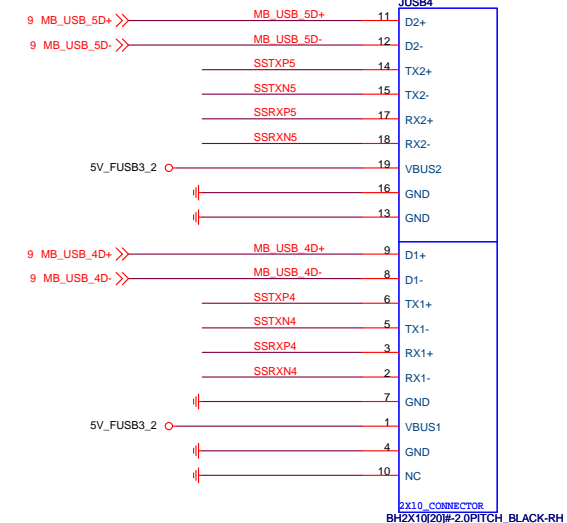
USB3.0: Re-driver to Connector Length < 5"

900 mA 900 mA
min 40mil. min 40mil.

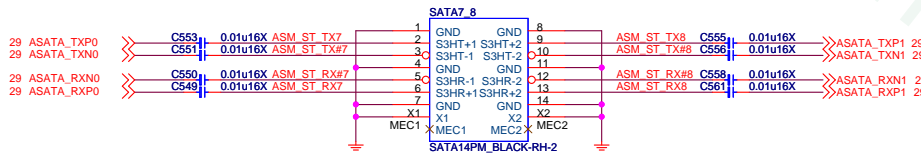
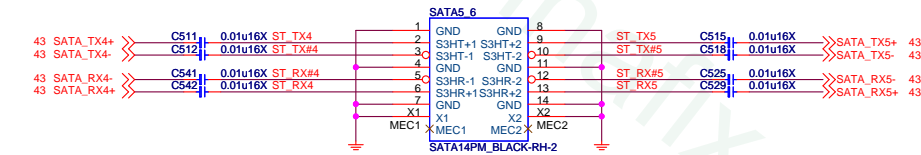
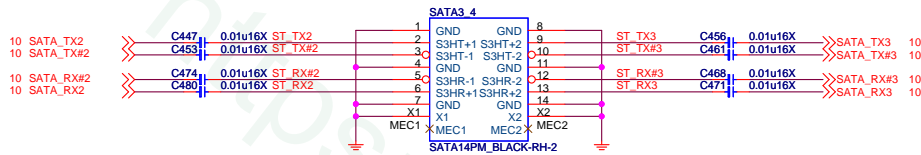
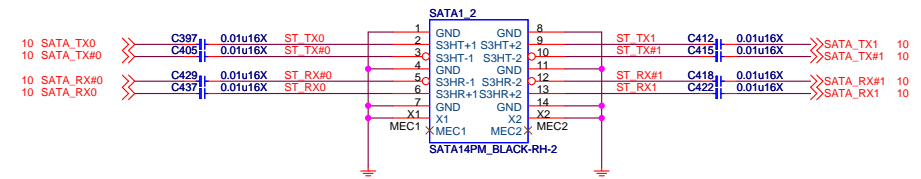


2014.03.10

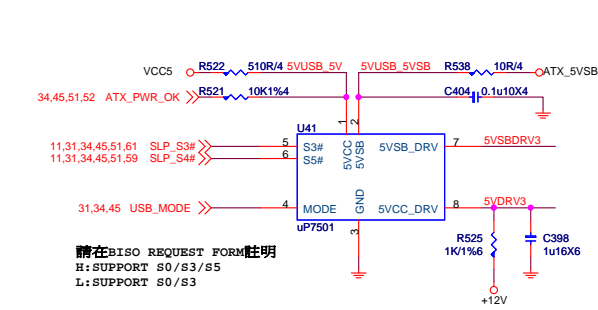
900 mA 900 mA
min 40mil. min 40mil.



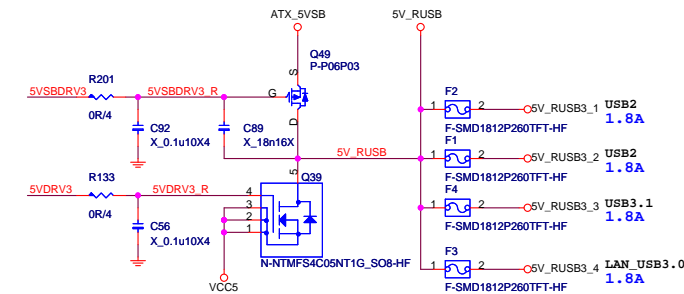
MICRO-STAR INT'L CO.,LTD			
MS-7888			
Size	Document Description	Rev	
Custom	INTEL USB3.0 Front Connector	11	
Date:	Tuesday, March 18, 2014	Sheet	41 of 68



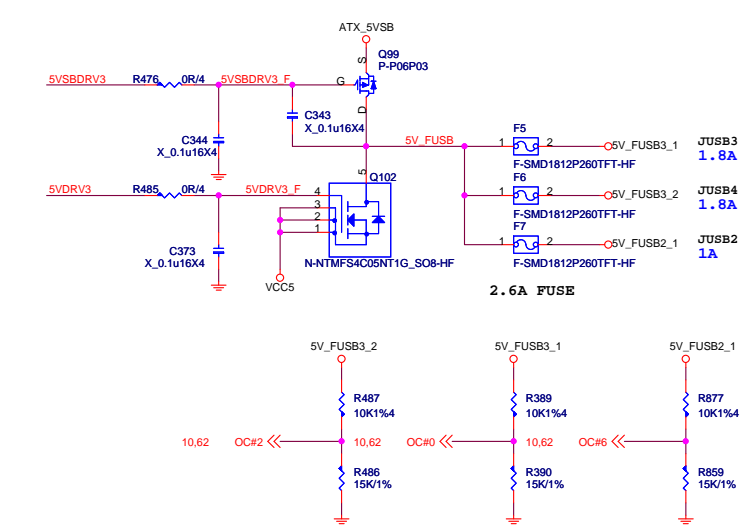
USB POWER



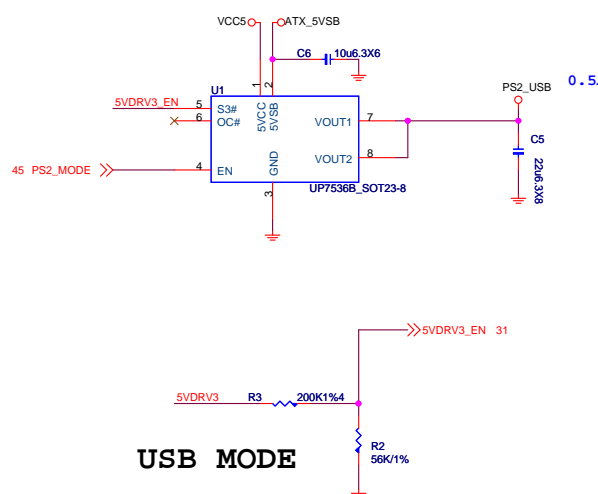
REAR USB PORT POWER



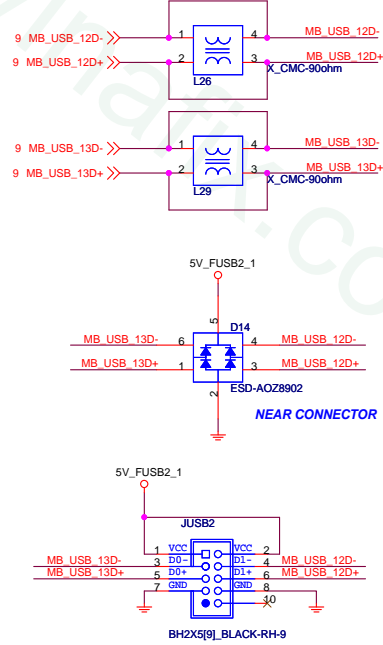
FRONT USB PORT POWER



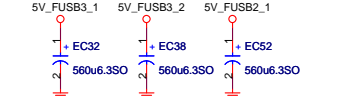
PS2 POWER



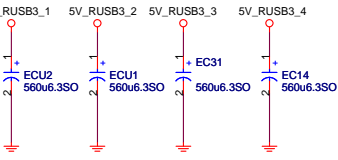
FRONT USB PORT 12,13

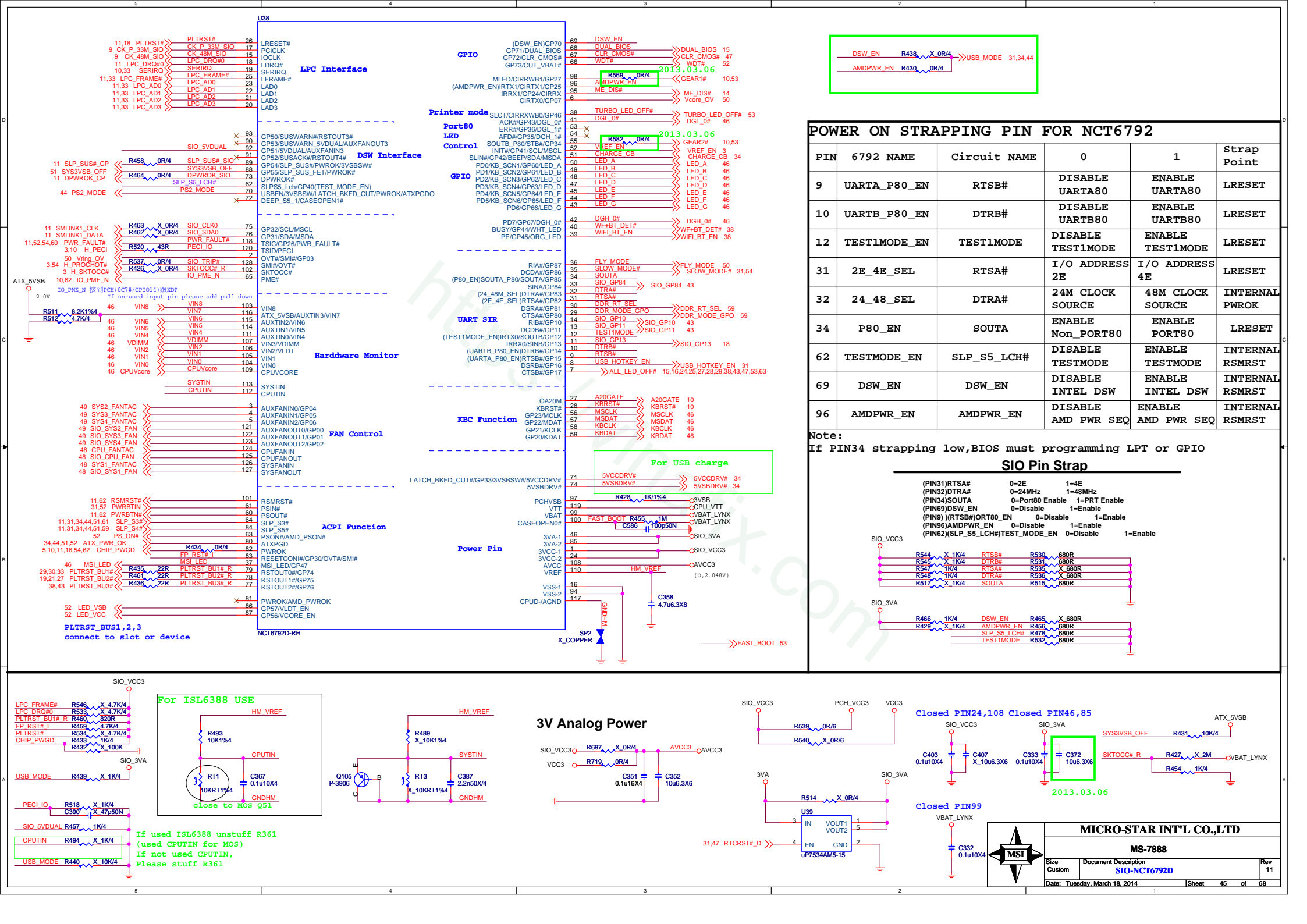


FRONT



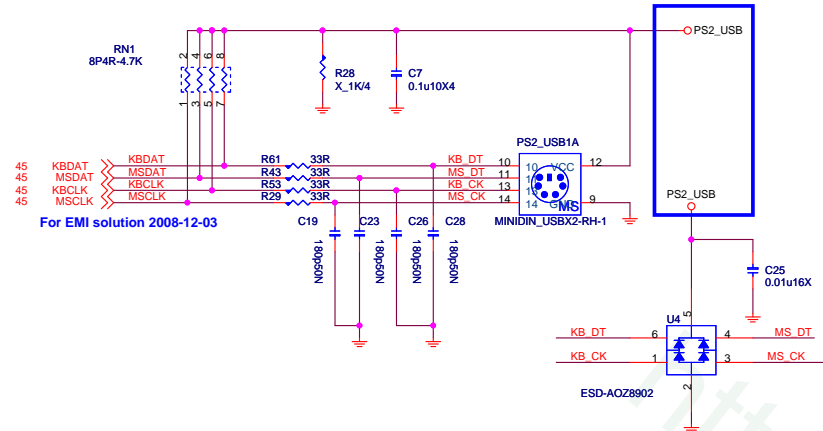
Real





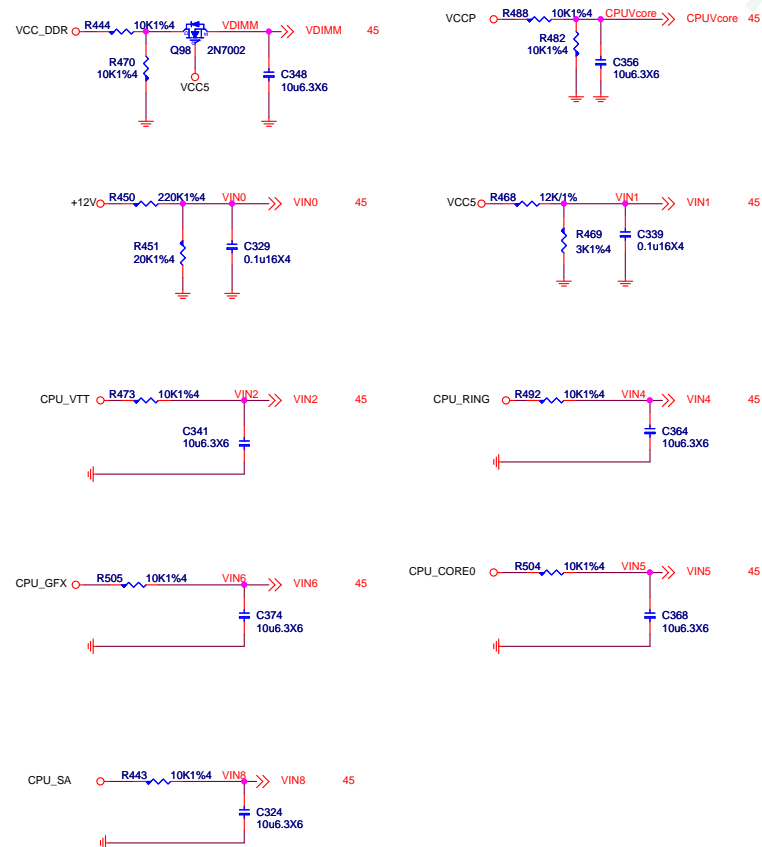
PS2 KEYBOARD & MOUSE CONNECTOR

可以切換在s5
底下是不是要有電

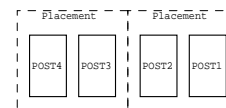


HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

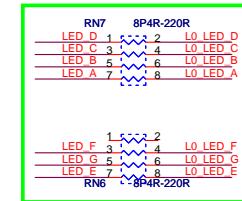


DEBUG LED



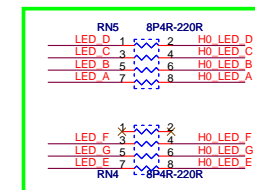
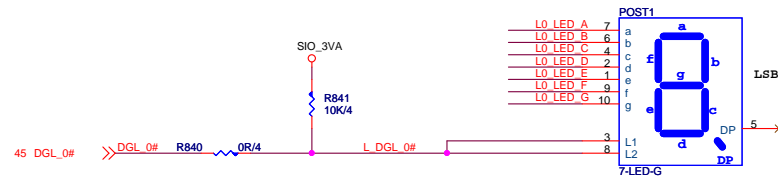
Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

45 LED_A
45 LED_B
45 LED_C
45 LED_D
45 LED_E
45 LED_F
45 LED_G

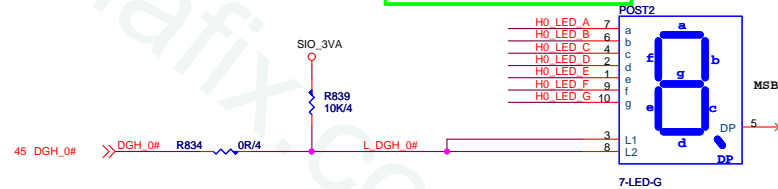


2014.03.12

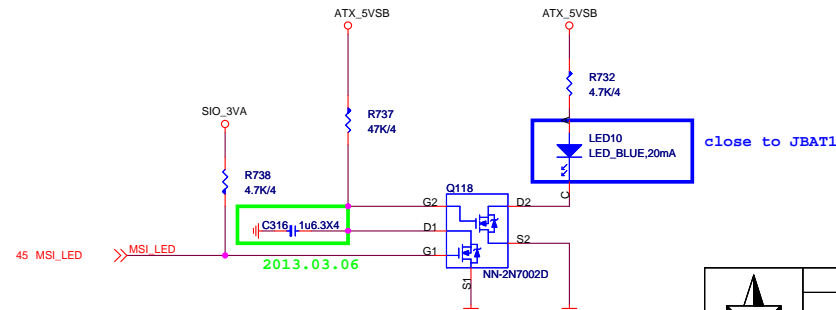
Debug LED OFF BIOS control



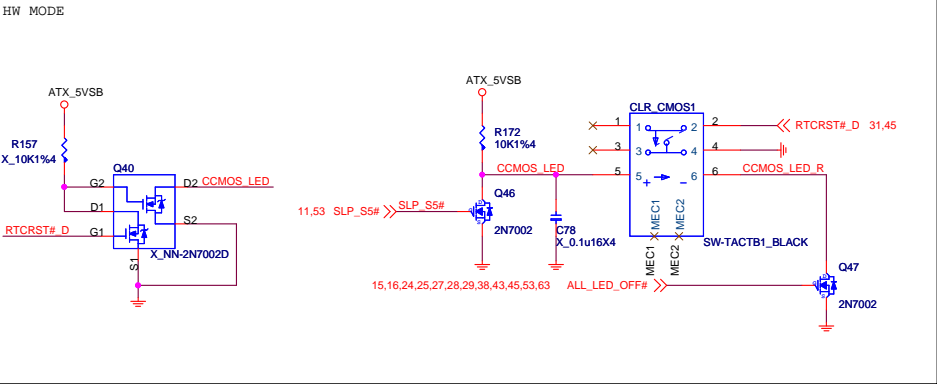
2014.03.12



MSI_LED



MICRO-STAR INT'L CO.,LTD		
MS-7799		
Size	Document Description	Rev
Custom	SIO-NCT6792D/PS2/Debug LED	11
Date: Tuesday, March 18, 2014	Sheet 46 of 68	



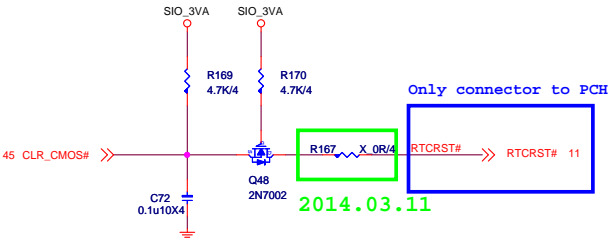
Clear CMOS button

LED LIGHTING RULE

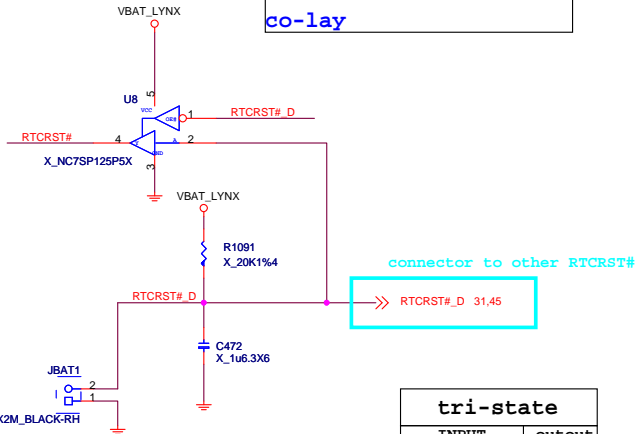
S0/S3/S4 : LED OFF

S5 : LED ON

BIOS MODE

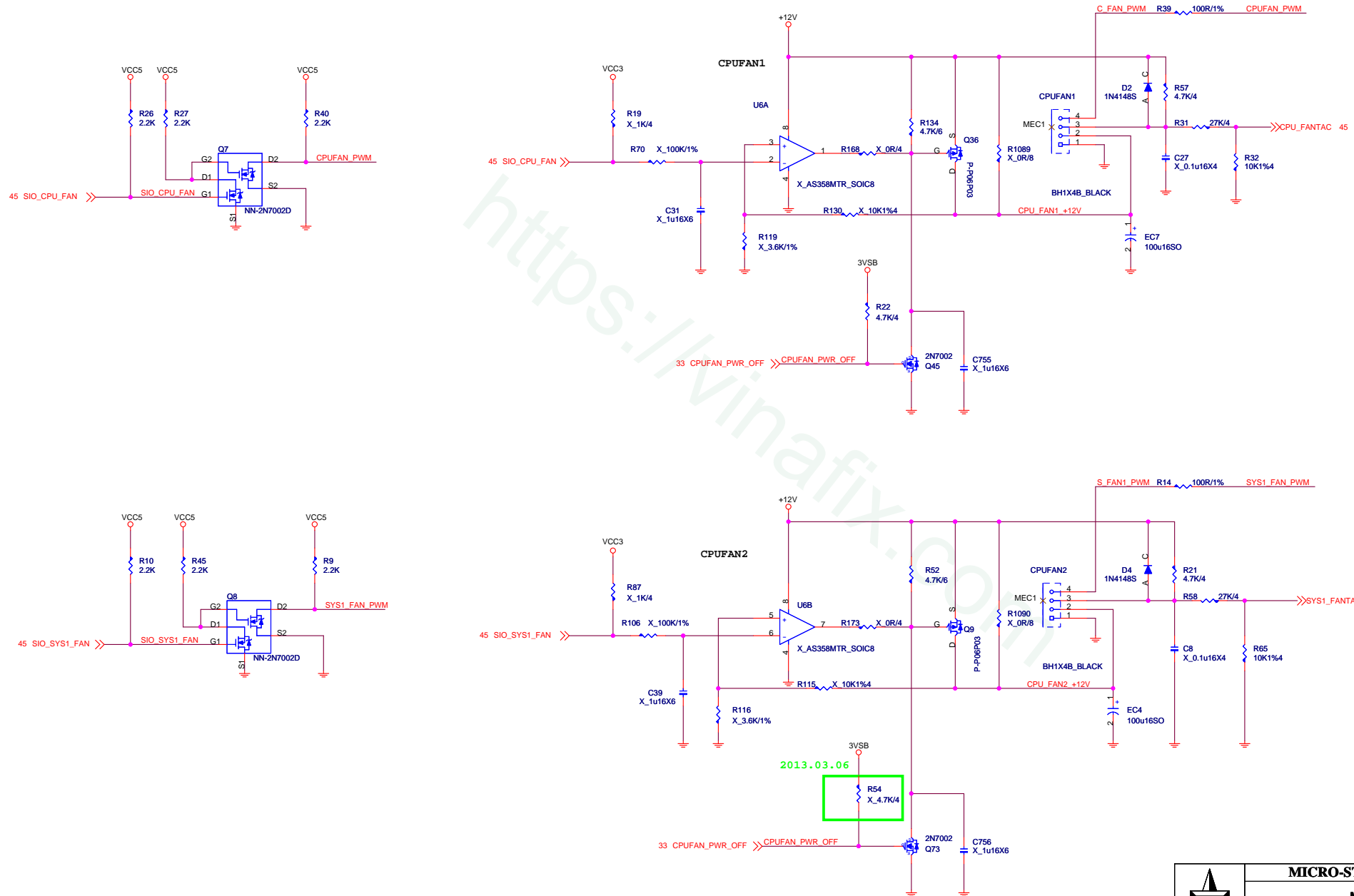


2014.03.11

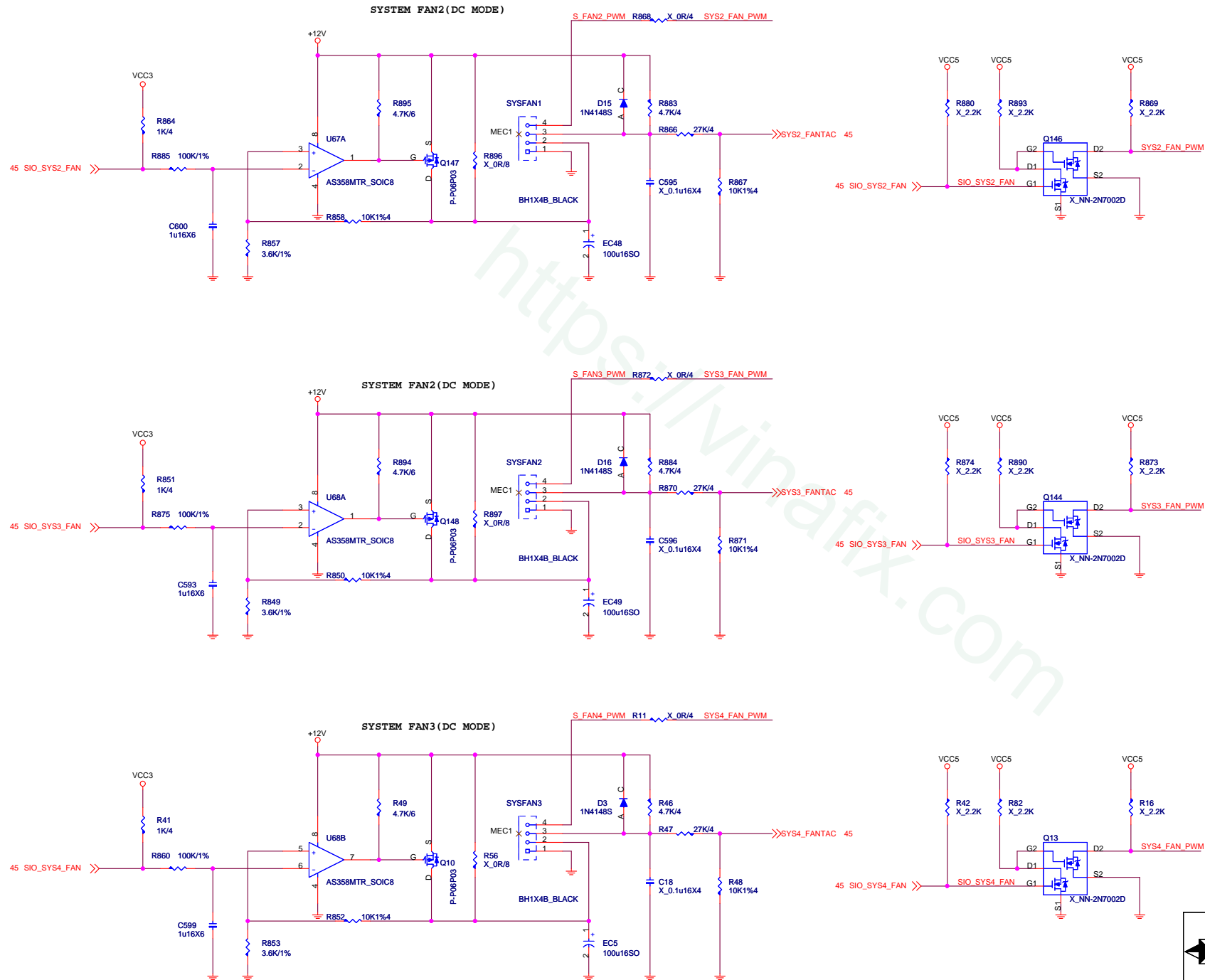


tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

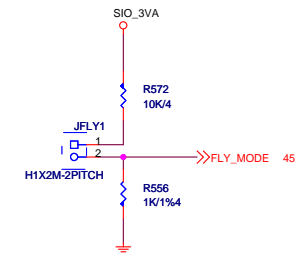
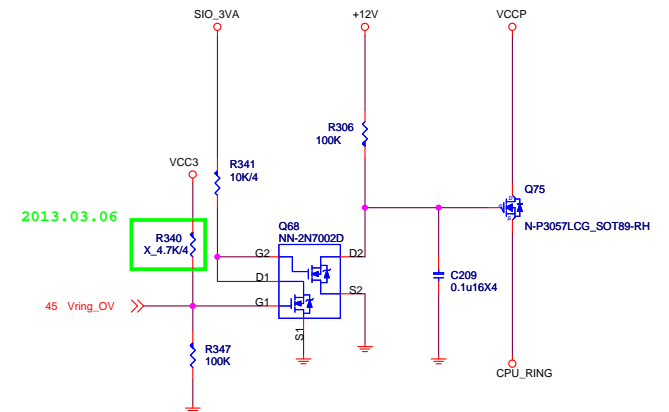
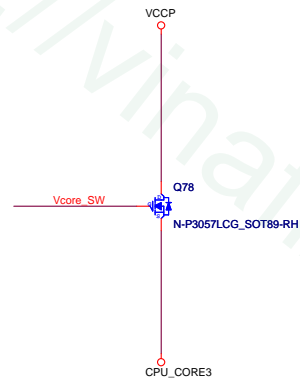
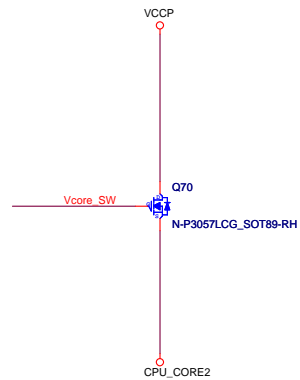
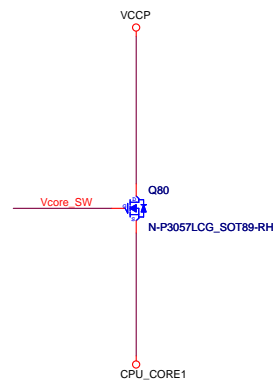
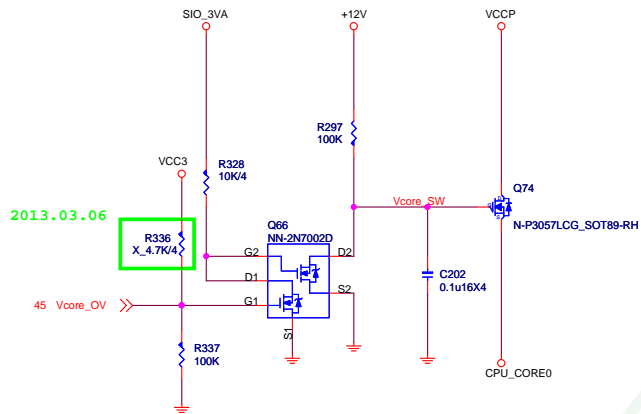
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



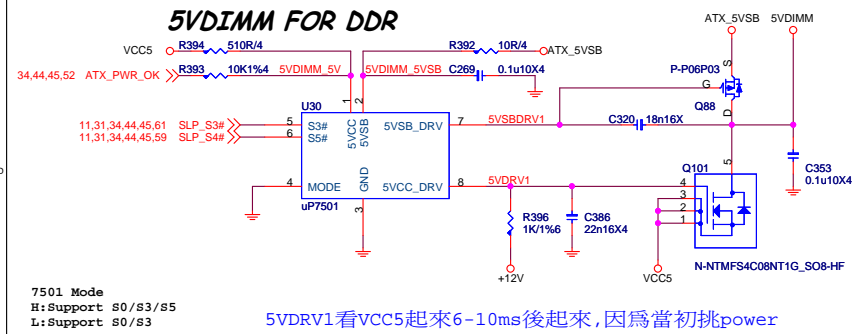
Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



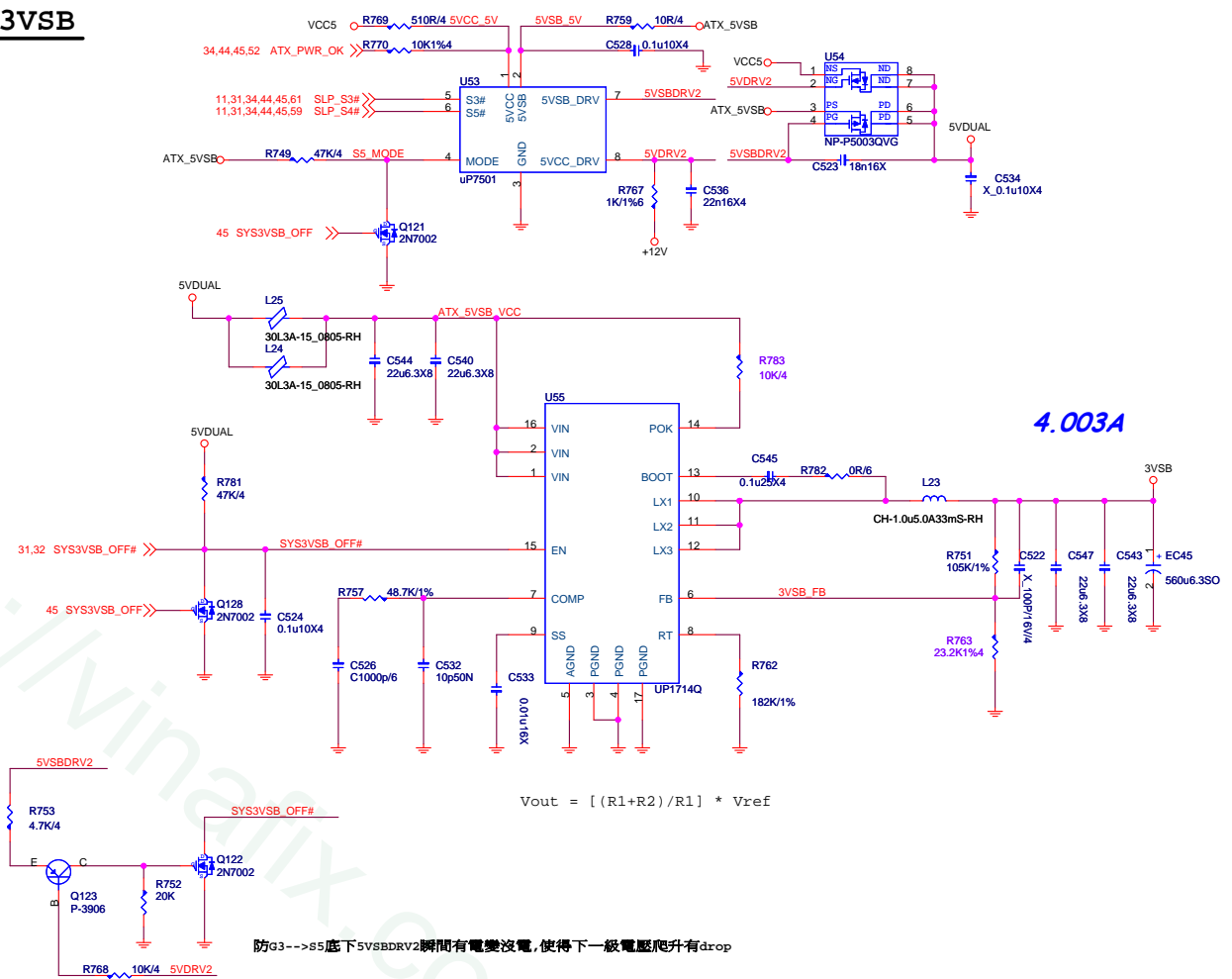
MICRO-STAR INT'L CO.,LTD		
MS-7888		
Size	Document Description	Rev
Custom	FAN CONTROLLER	11
Date: Tuesday, March 18, 2014	Sheet 49 of 68	



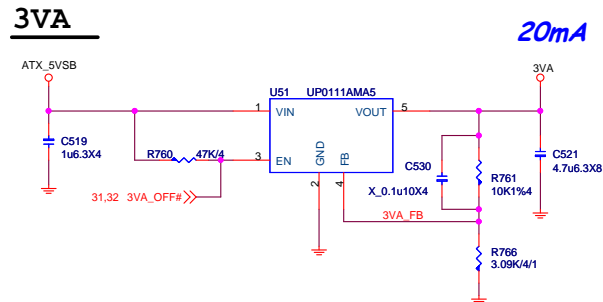
5VDIMM FOR DDR



3VSB



3VA

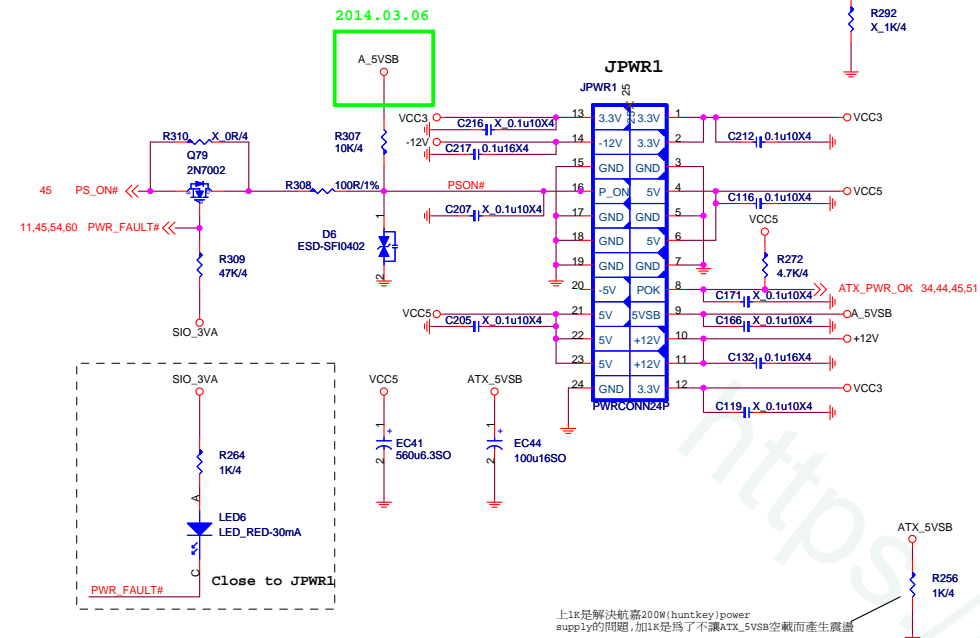


MICRO-STAR INT'L CO.,LTD

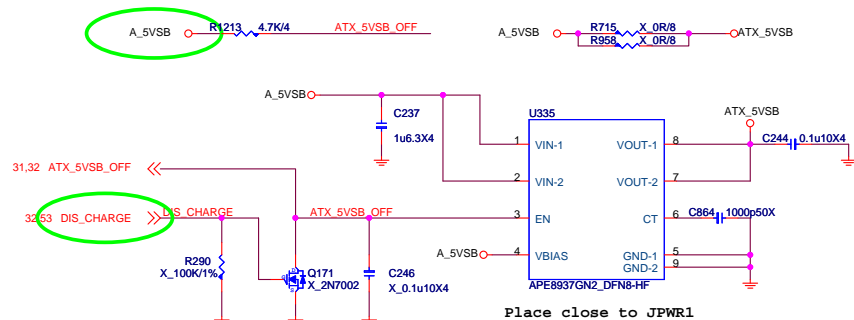
MS-7888

Size	Document Description	Rev
Custom	ACPI Controller UPI	11
Date: Tuesday, March 18, 2014	Sheet 51 of 68	

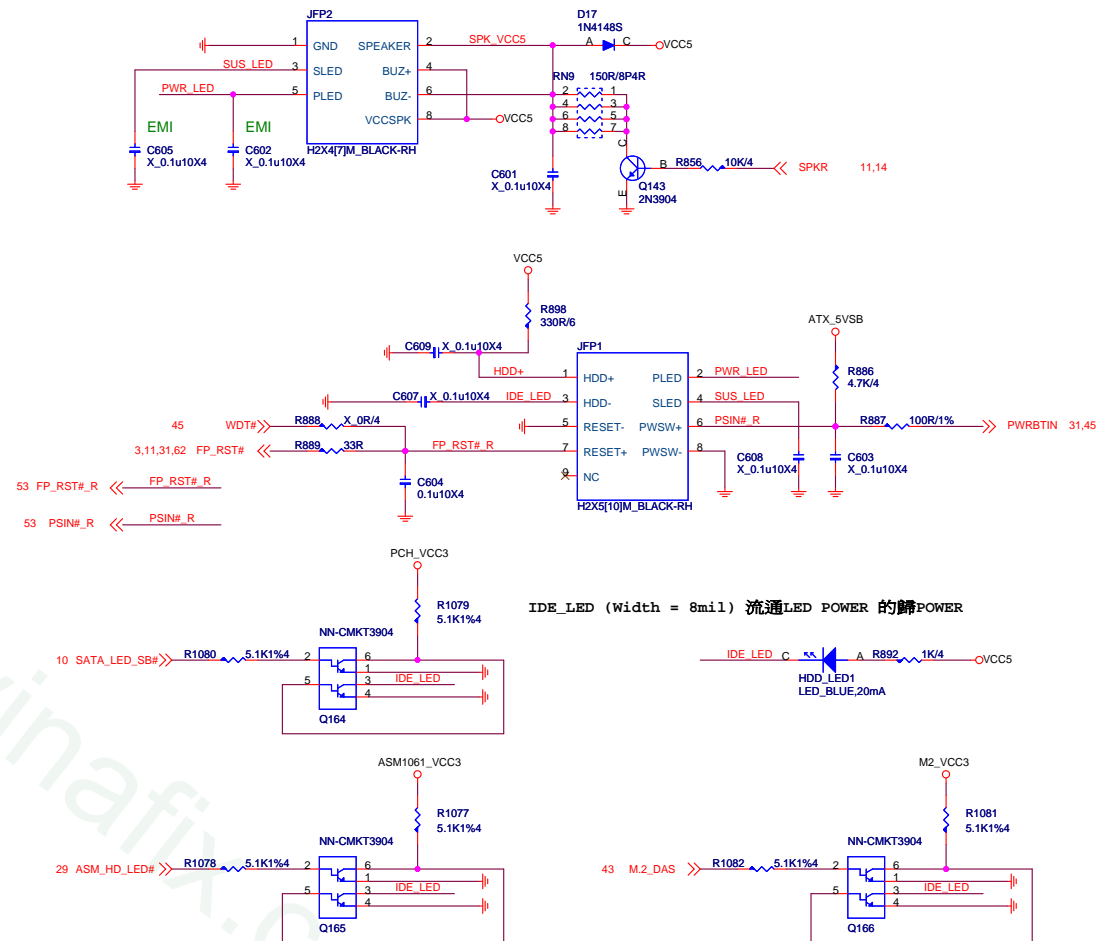
ATX POWER CONNECTOR



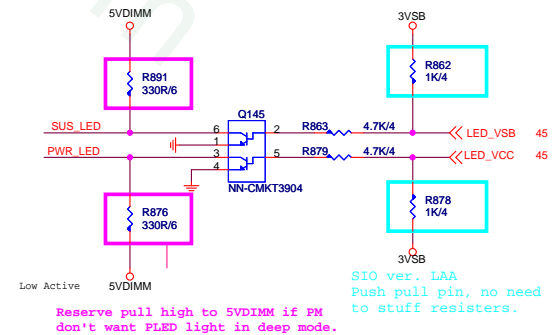
放電的時候SIO有漏電
為了防止ATX_5VSB漏電的問題
多加一組ATX_5VSB-->5VSB防漏電的線路
這個線路請放在ATX CONNECT一出來的地方



FRONT PANNEL



Front Panel LED

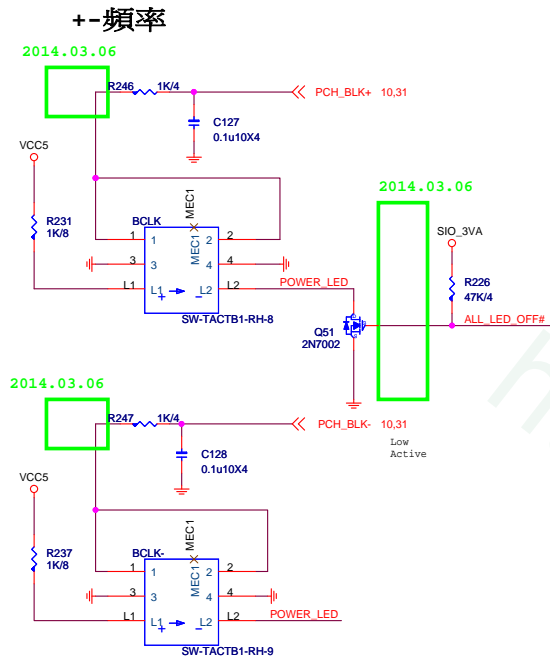


MICRO-STAR INT'L CO.,LTD

MS-7888

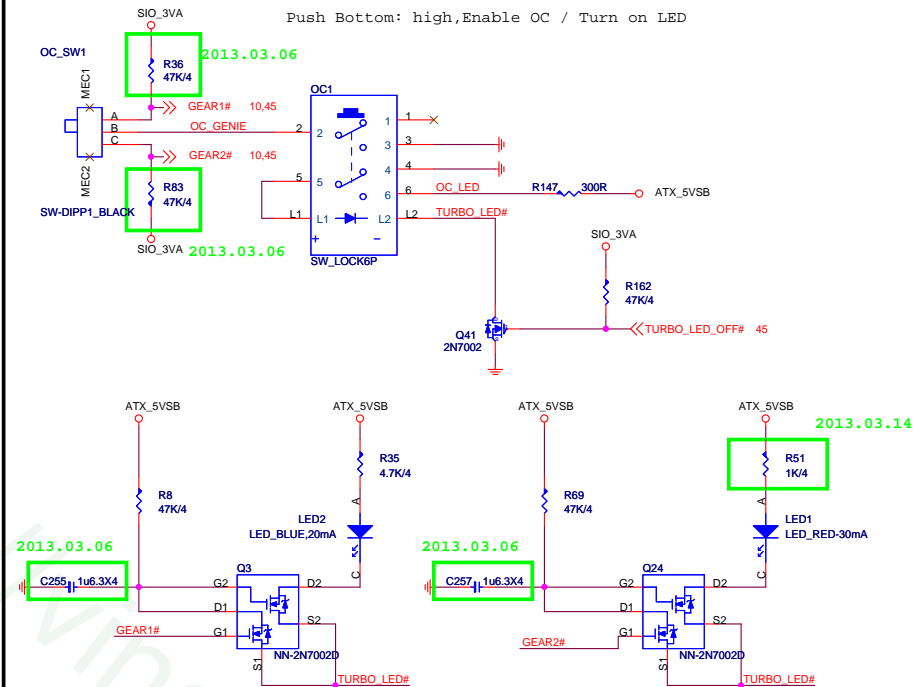
Size	Document Description	Rev
Custom	ATX F_Panel/TPM/JDLED4	11
Date:	Tuesday, March 18, 2014	Sheet 52 of 68

Turbo Button

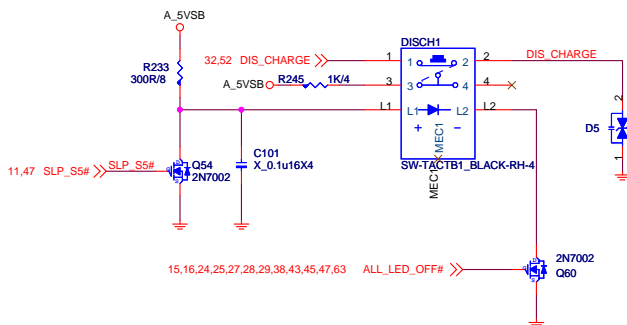


TURBO_MODE#

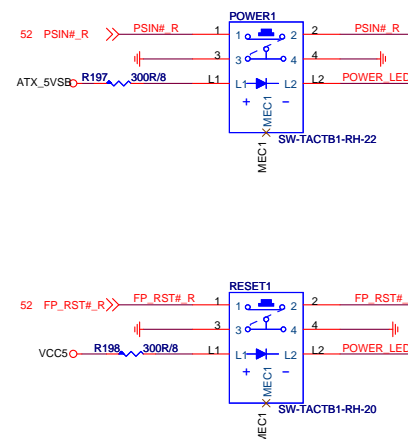
TURBO_MODE#
Default: Low,disable OC
Push Bottom: high,Enable OC / Turn on LED



Discharge Botton



PWR/RST Botton



Fast boot Button

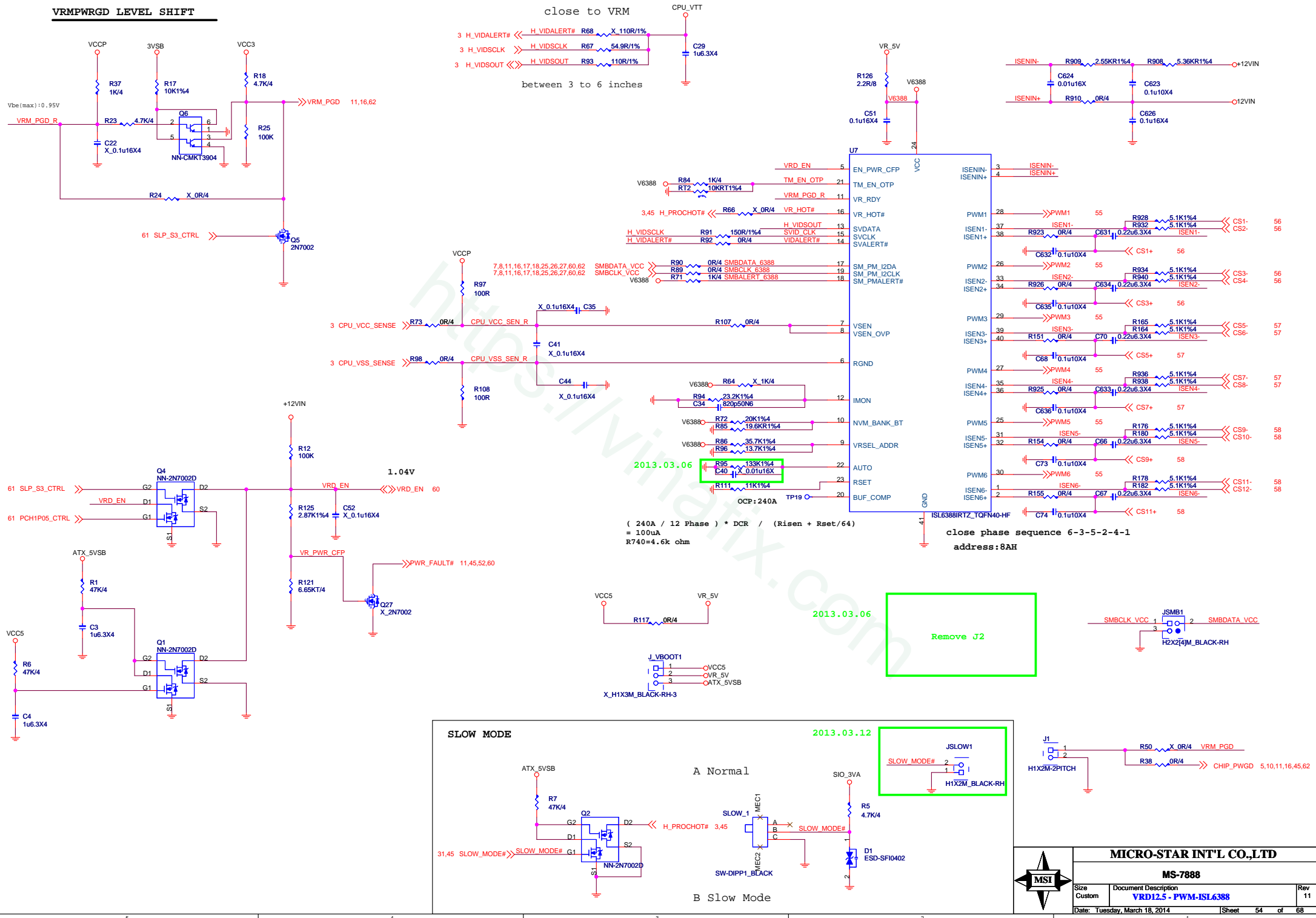


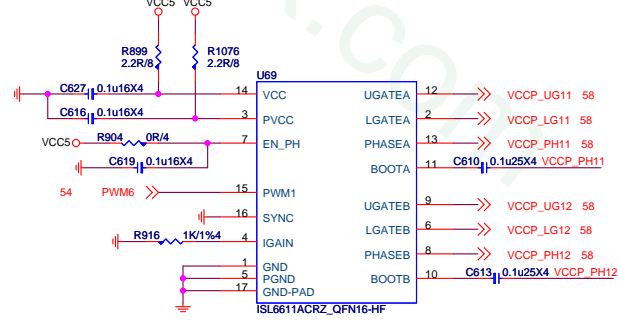
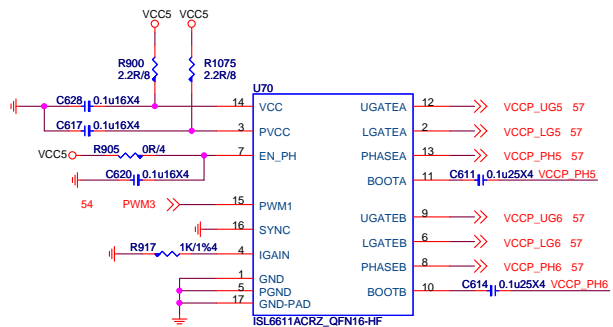
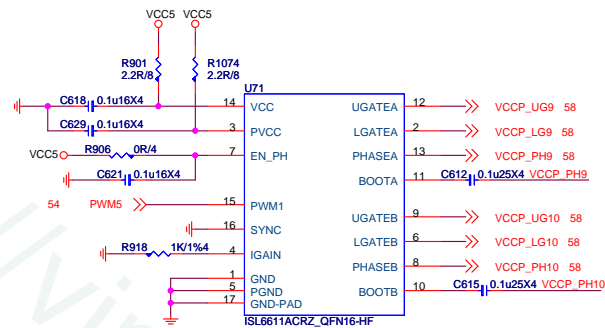
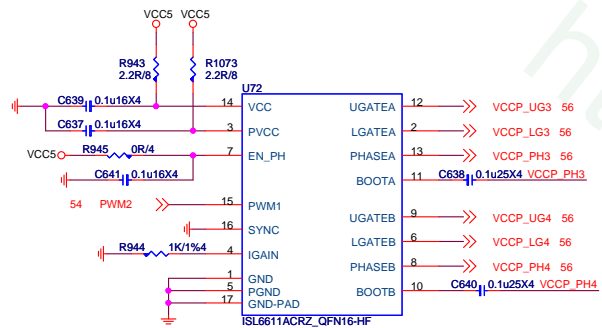
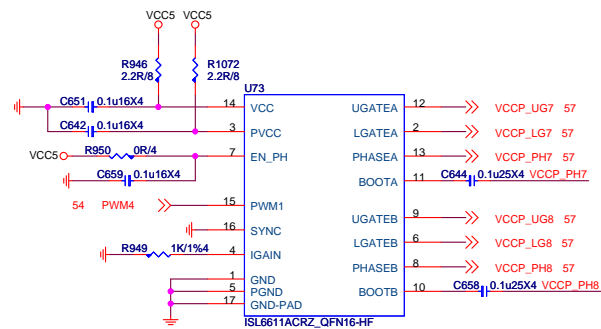
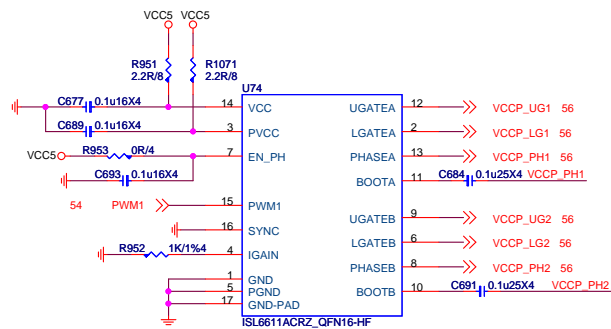
MICRO-STAR INT'L CO.,LTD

MS-7888

Size	Document Description	Rev
Custom	BUTTON	11
Date: Tuesday, March 18, 2014	Sheet 53 of 68	

VRMPWRGD LEVEL SHIFT

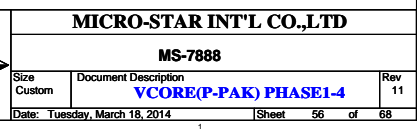


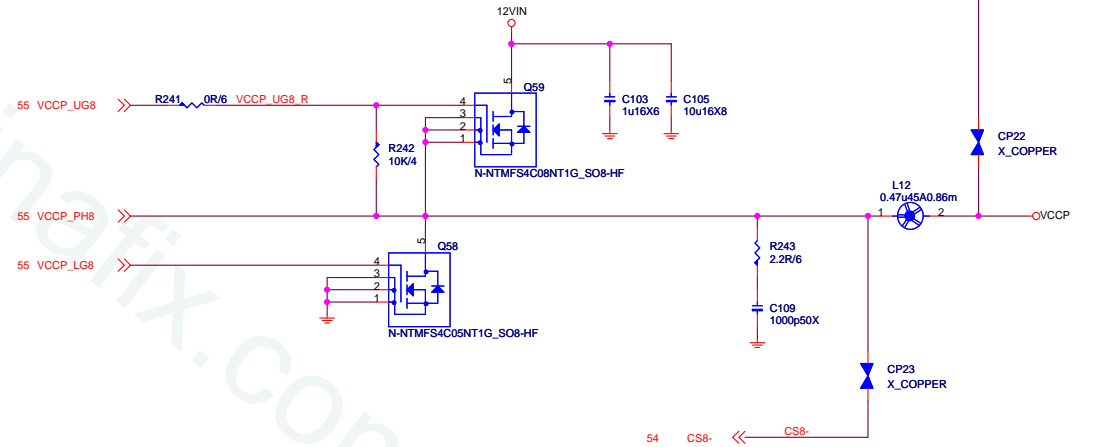
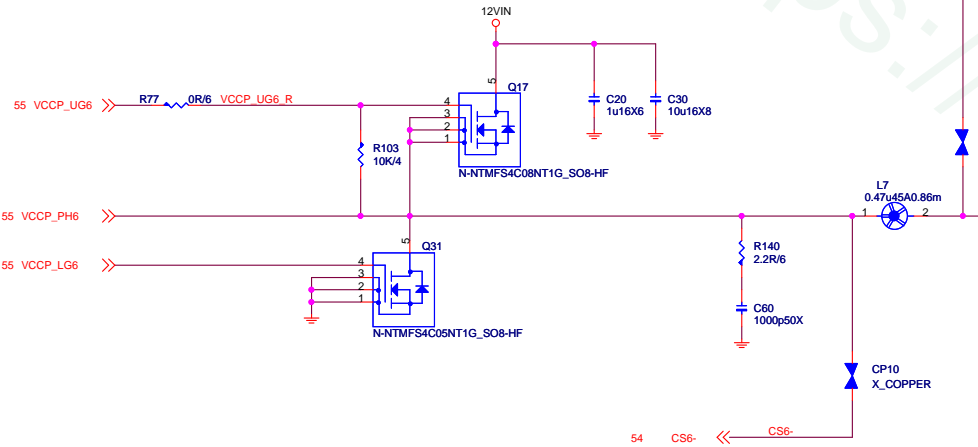
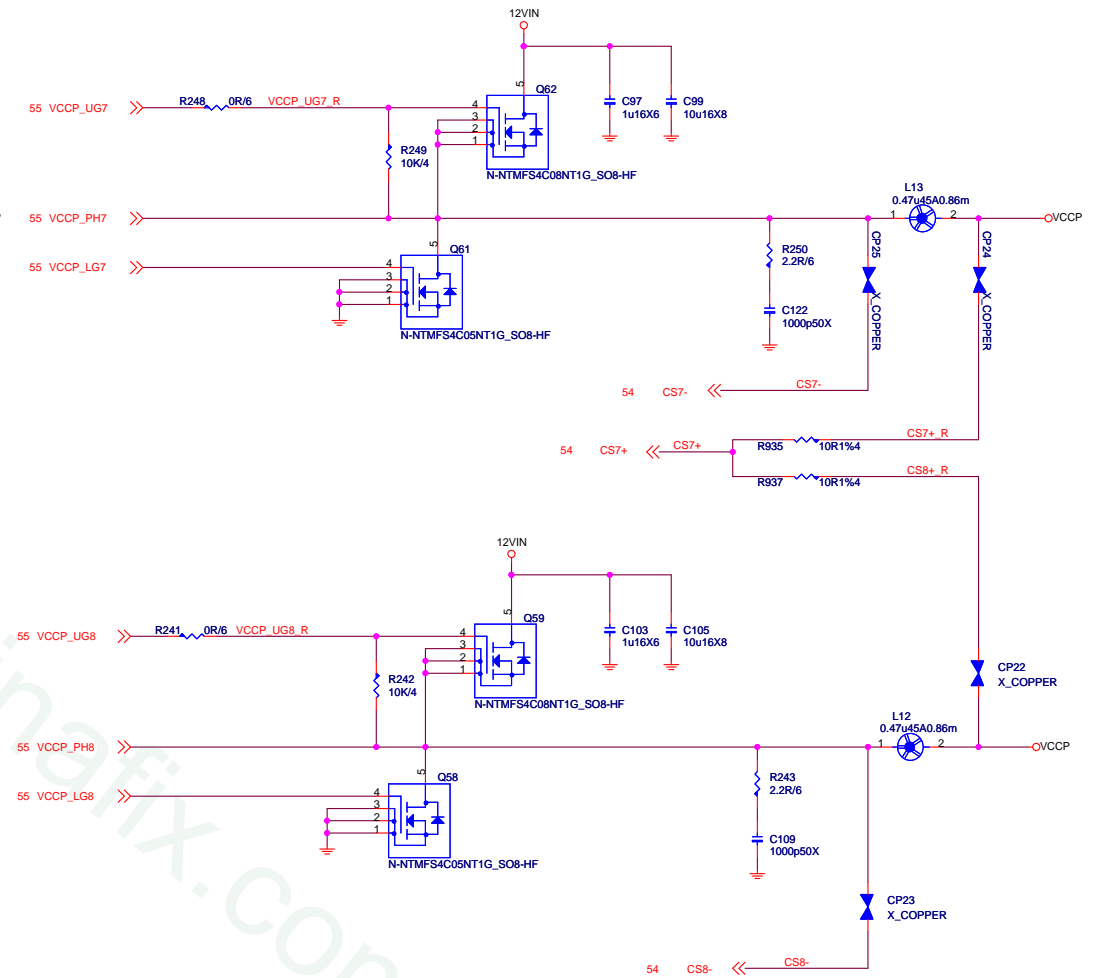
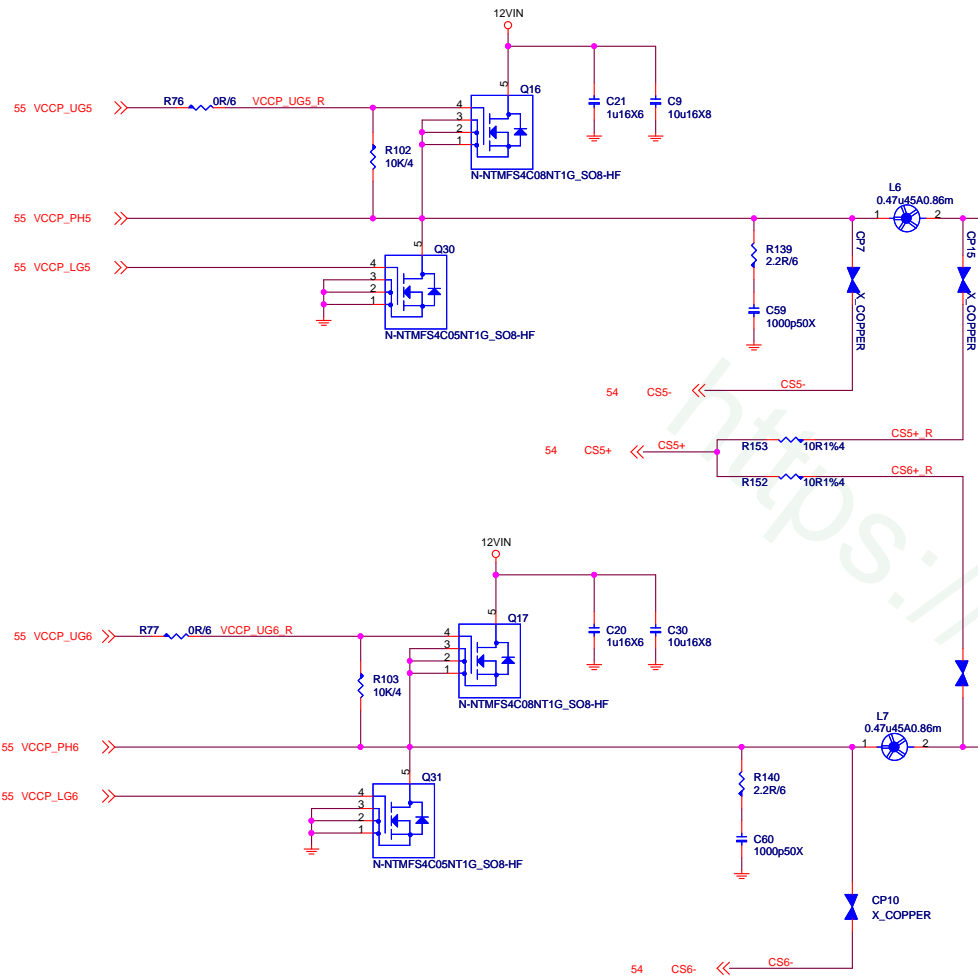


MICRO-STAR INT'L CO.,LTD

MS-7888

Size	Document Description	Rev
Custom	ISL6617+ISL6611 PHASE1-8	11
Date: Tuesday, March 18, 2014	Sheet 55 of 68	

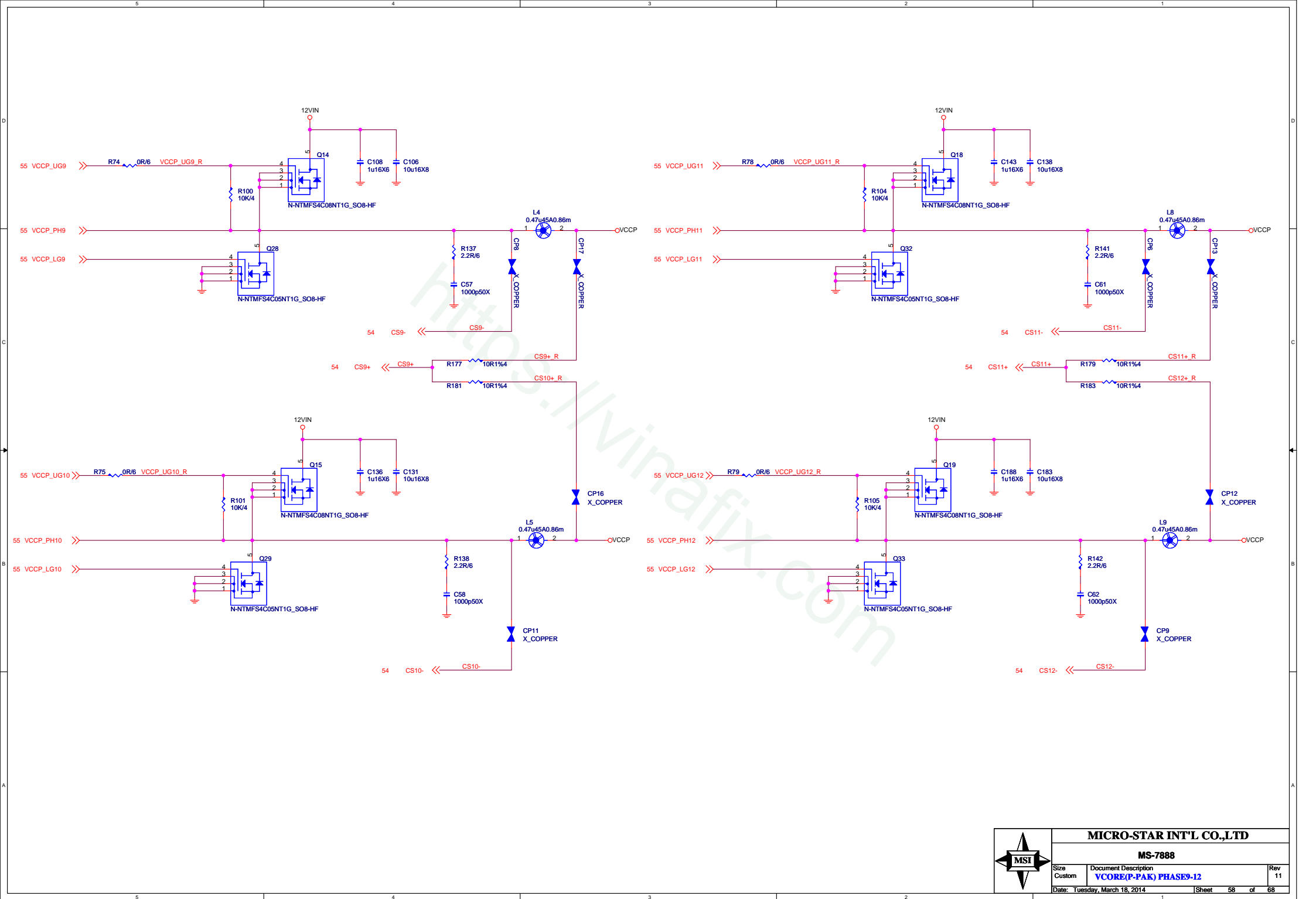




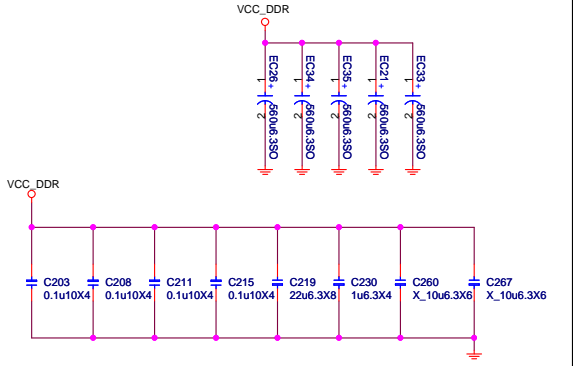
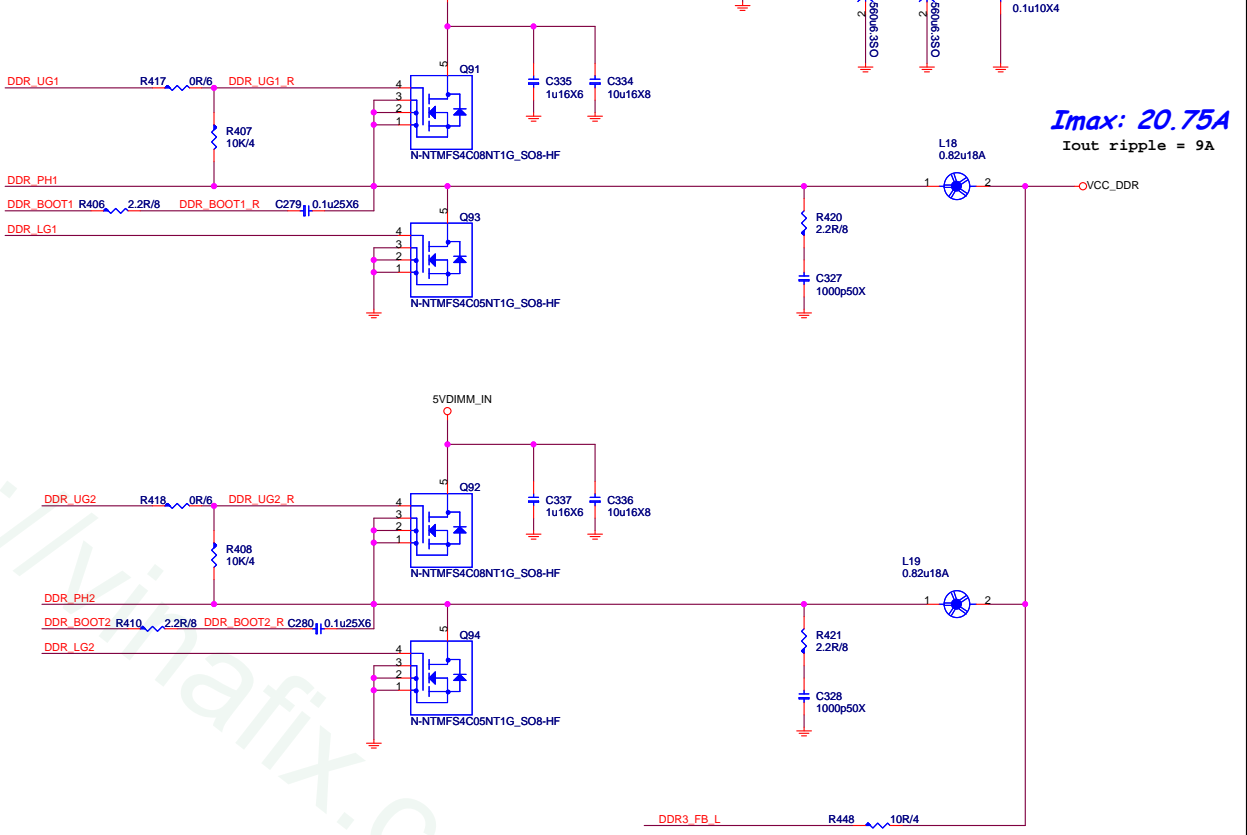
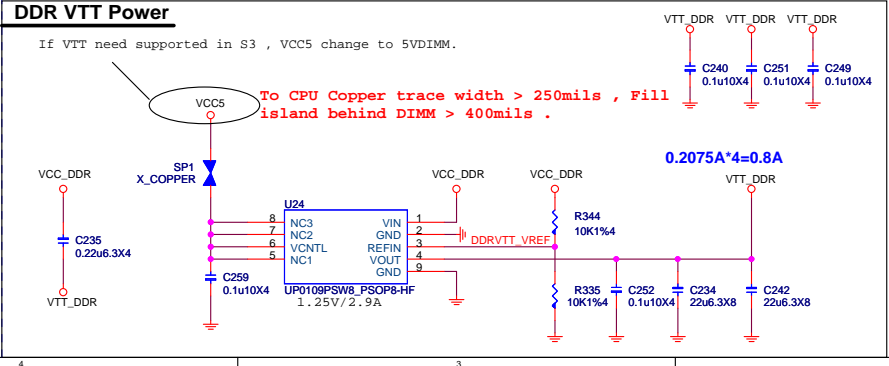
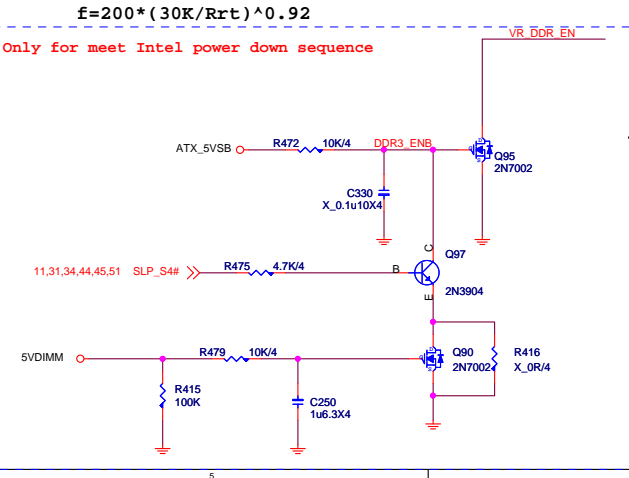
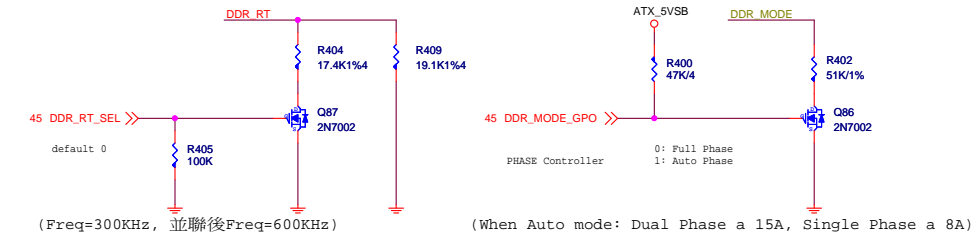
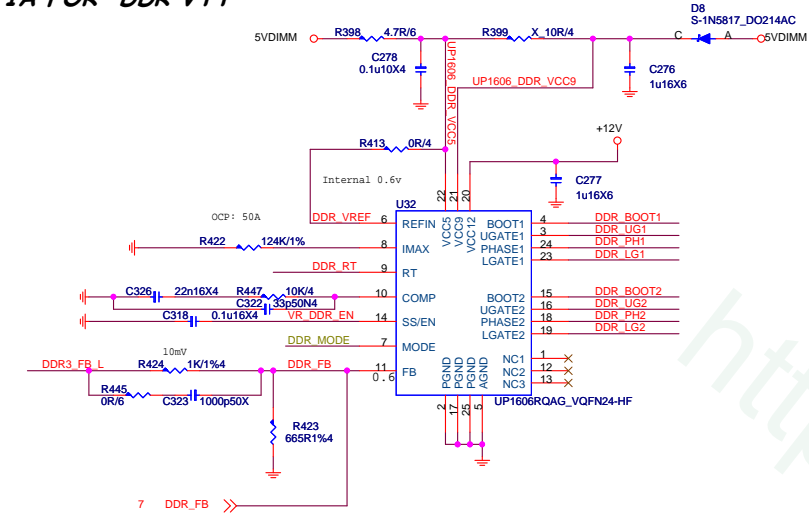
MICRO-STAR INT'L CO.,LTD

MS-7888

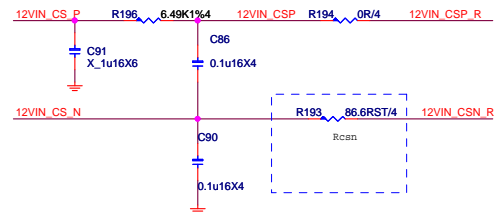
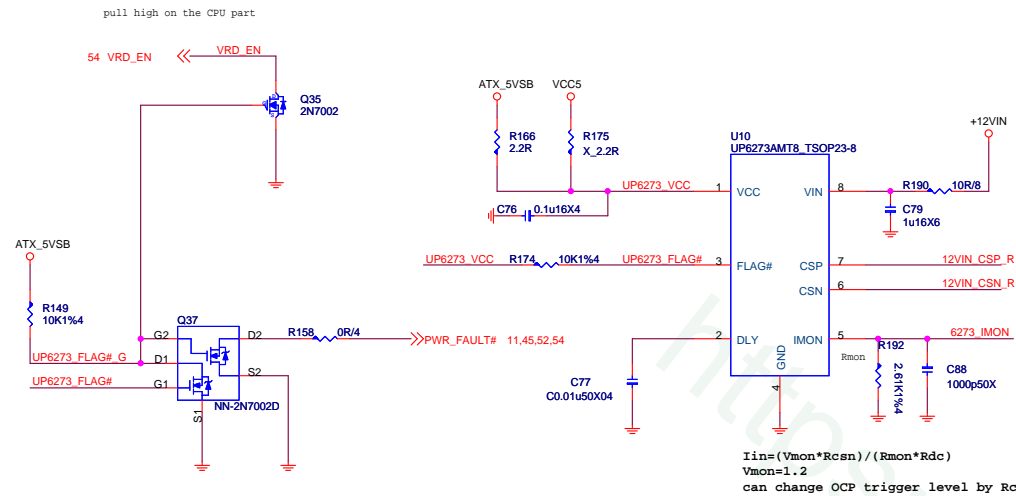
Size Custom	Document Description VCORE(P-PAK) PHASE5-8	Rev 11
Date: Tuesday, March 18, 2014	Sheet 57	of 68



DDR3_1.5V 4.75A+15A+1A=20.75A
4.75A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

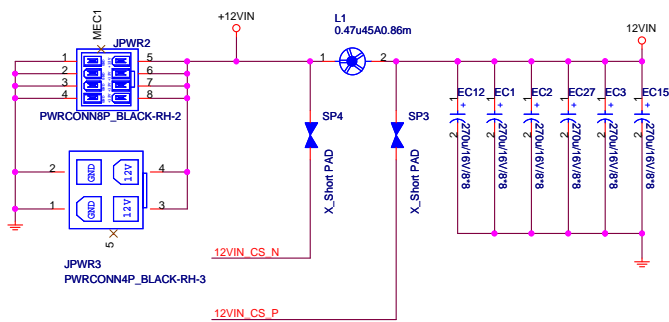


POWER METER



UPI VOLTAGE CONSOLE

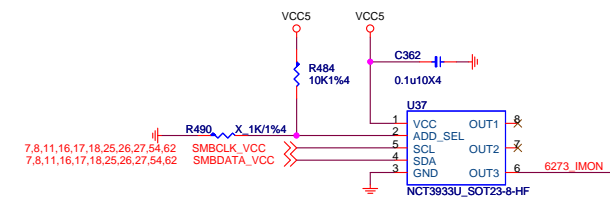
0xD4:RL=10K												
ADDRESS	0xD4			0xD6			0xD8			0xDA		
	Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max
BUS_SEL Viotage	70	90	110	170	210	250	310	380	450	510	600	690



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

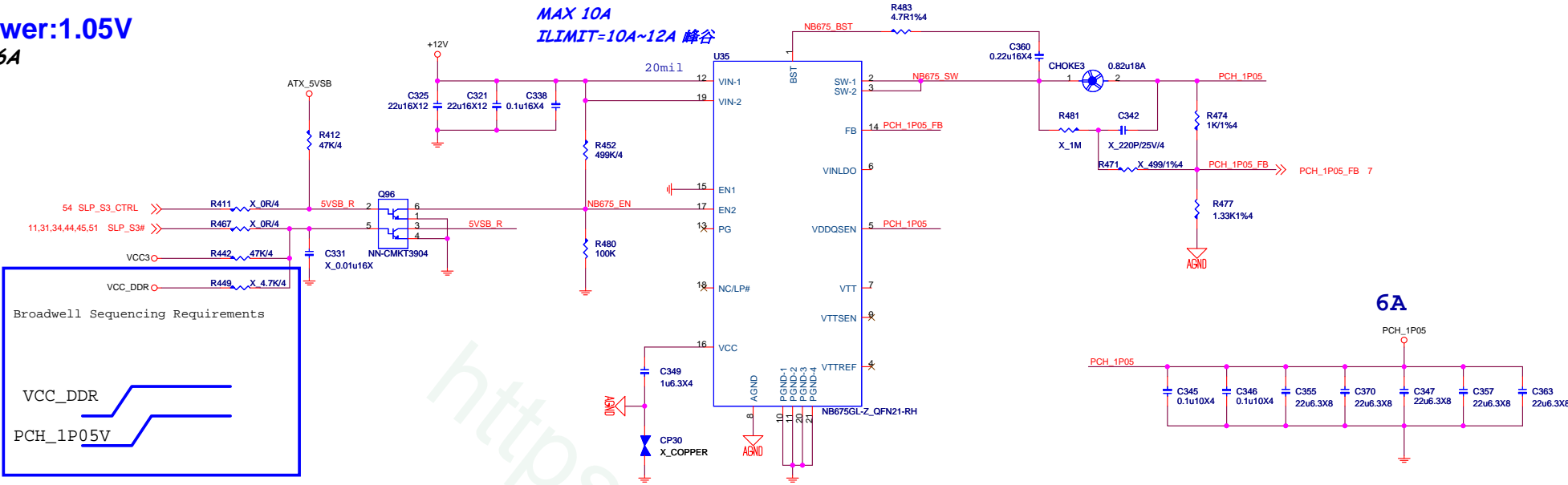


MICRO-STAR INT'L CO.,LTD

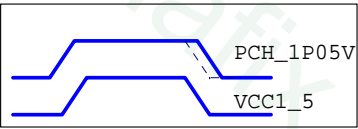
MS-7888

Size Custom	Document Description 12VIN CURRENT SENSE	Rev 11
Date: Tuesday, March 18, 2014		Sheet 60 of 68

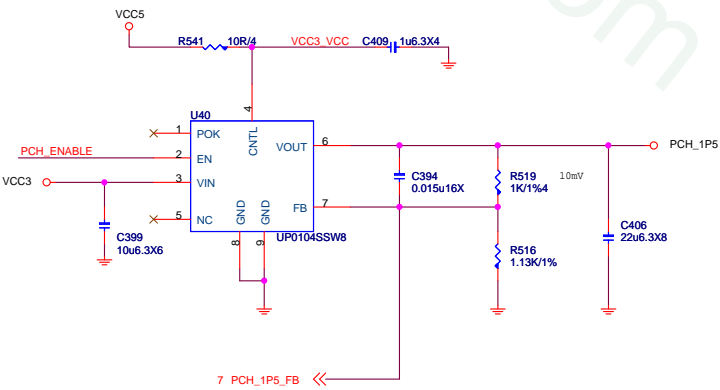
PCH Power:1.05V
PCH Core 6A



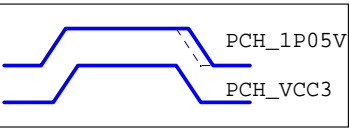
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



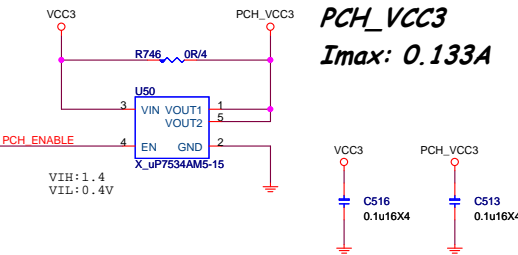
PCH_1P5
Imax: 0.35A



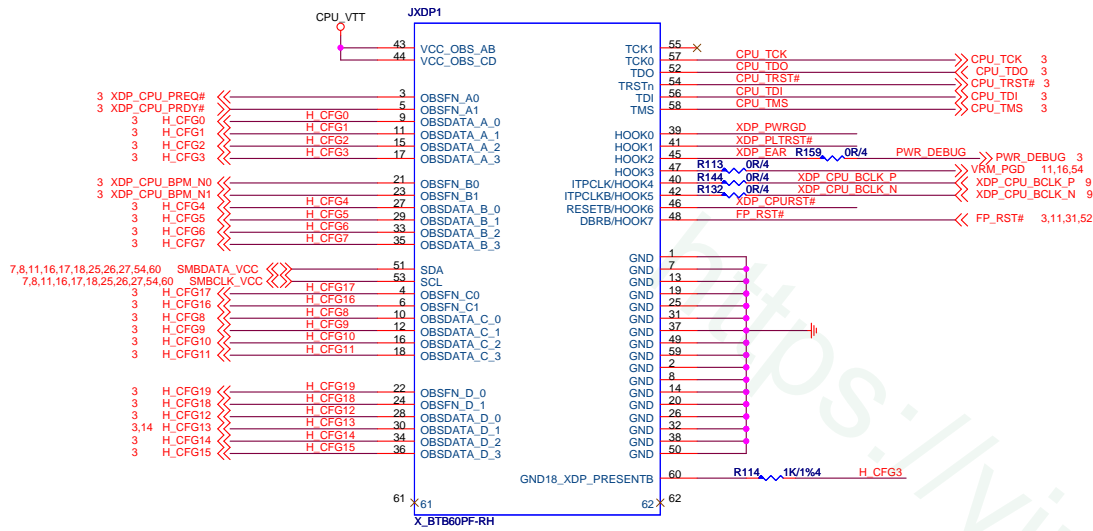
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



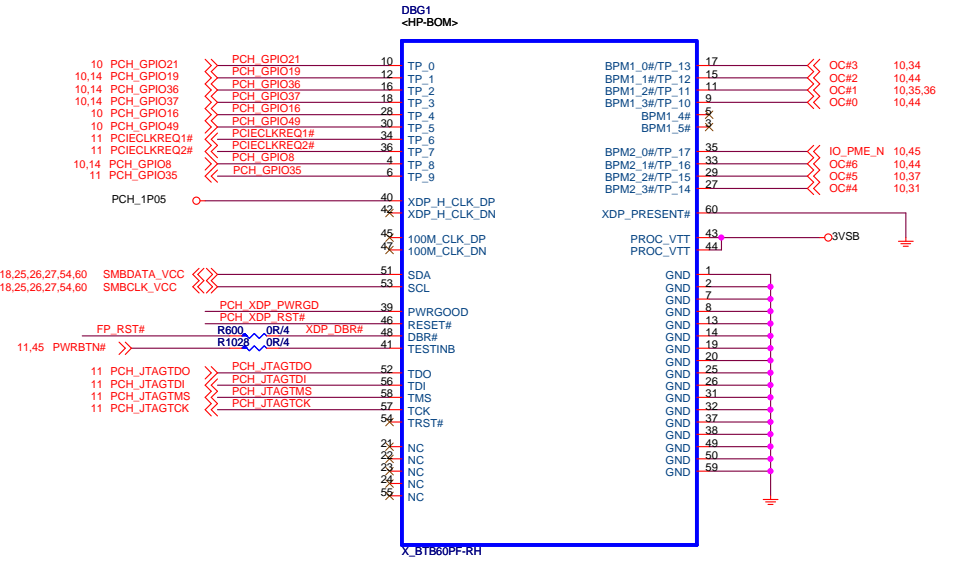
PCH_VCC3
Imax: 0.133A



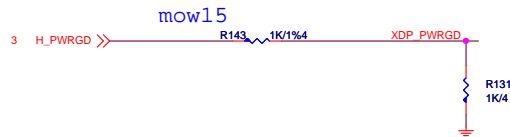
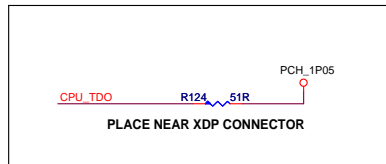
Reserve debug port 5020



PCH XDP



Not unstuff for CPU_TDO pull high



11,45 PWRBTN# >> R185 0R/4 XDP_PLTRST#

3,11 CPURST# >> R129 1K/4 XDP_CPURST#

PCH XDP PWRGD/RESET

5,10,11,16,45,54 CHIP_PWGD >> R1018 1K/1%4 PCH_XDP_RST#

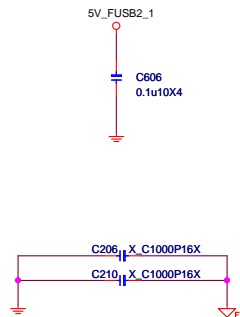
PCH_XDP_PWRGD >> R688 1K/1%4 RSMRST# << RSMRST# 11,45



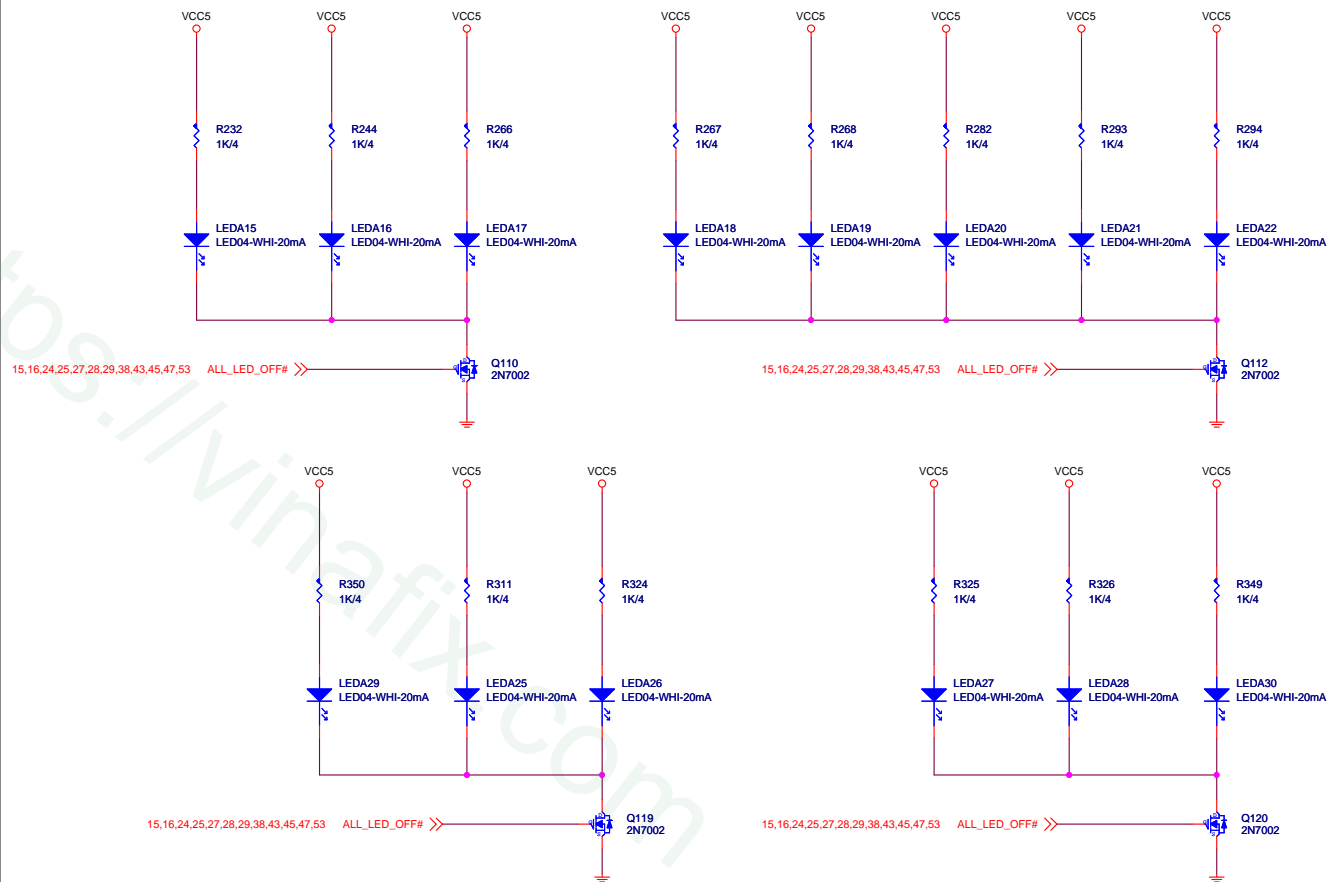
MICRO-STAR INT'L CO.,LTD

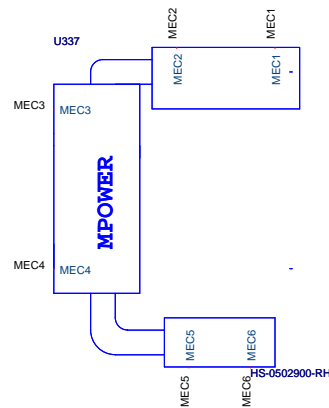
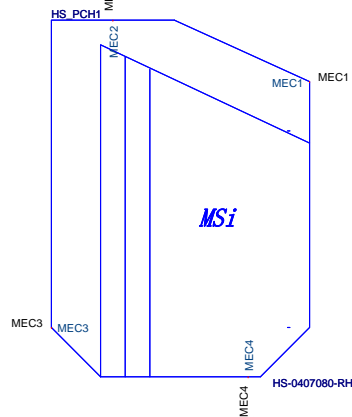
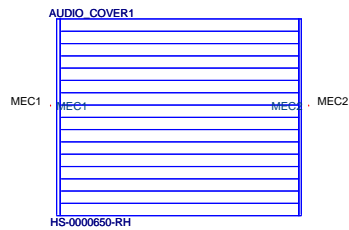
MS-7888

Size	Document Description	Rev
Custom	XDP CPU & PCH	11
Date: Tuesday, March 18, 2014	Sheet 62 of 68	

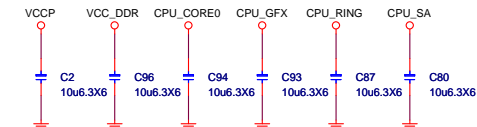
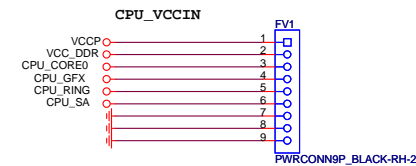


AUDIO Moat LED



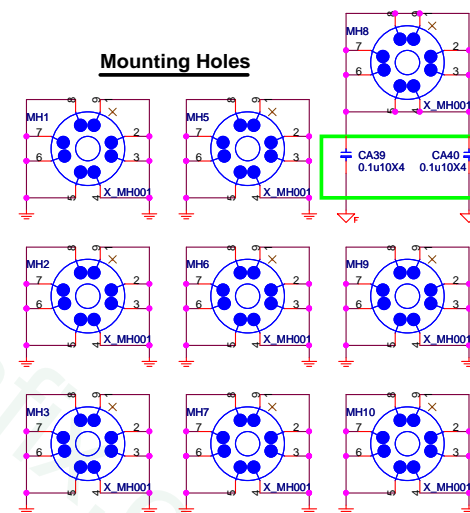


Voltage test point

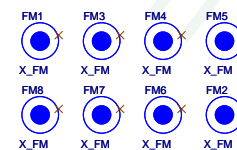


2013.03.06

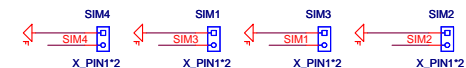
Mounting Holes



Optical Fiducial Marks-120



Simulation



2014/3/142014/3/21PD0-0788811-G37,精成,23,寶安恩斯邁廠(MSIS)
2014/3/142014/3/21PD0-0788811-G37,精成,52,寶安恩斯邁廠(MSIS)
2014/3/142014/3/21PD0-0788811-E48,競華,23,寶安恩斯邁廠(MSIS)
2014/3/142014/3/21PD0-0788811-E48,競華,52,寶安恩斯邁廠(MSIS)